PROGRAMME

MONDAY 4 MARCH, 2002

0730	TUTORIAL REGISTRATION	
0800		Tutorial Breakfast
0930		
A1	Room A	**System Level Specification Beyond RTL**
B1	Room B	**Low Power/Low Energy Embedded Software**
C1	Room C	**Test Resource Partitioning Strategies for SoC**
E1	Room E	**Design Methodologies and CAD Tools for Mixed-Signal and RF Ics**
1430		
A2	Room A	**Platform Based Design**
B2	Room B	**Low Power Hardware Design**
C2	Room C	**Design and Testing Challenges for Low-Voltage Scaled CMOS Circuits**
E2	Room E	**Test-Based Methods for Design Verification and Diagnosis**

Tutorial attendees should choose in advance one tutorial from A1, B1, C1 or E1 which take place in the forenoon and one tutorial from A2,B2,C2 or E2 which take place in the afternoon.
The topics will run in parallel with the following timescale.
Rooms will be signposted.

0730 - 0930	Registration and Tutorial Breakfast
0930 – 1100	Tutorials – Level 2
1100 – 1130	Break
1130 – 1300	Tutorials – Level 2
1300 – 1430	Lunch – Level 4
1330	CONFERENCE REGISTRATION BEGINS
1430 – 1600	Tutorials – Level 2
1600 – 1630	Break
1630 – 1800	Tutorials – Level 2
1800 – 1930	WELCOME RECEPTION – Level 2
1900 – 2100	FRINGE TECHNICAL MEETINGS

TUESDAY 5 MARCH, 2002

0730 **REGISTRATION CONTINUES**

PLENARY – OFFICIAL OPENING

Blue Room – Level 2

Session Chairman: J da Franca, ChipIdea, PT

0900 **OPENING REMARKS**
J da Franca, General Chair, ChipIdea, PT
C Delgado Kloos, Programme Chair, U Carlos III de Madrid, ES

Presentation of EDA Consortium, Phil Kaufman Award, by R Bingham, Cadence Design Systems, US

Best Paper Awards by P Quinton, IRISA, FR

Best Papers from DATE 2001 were:-

Track A: TRACE-DRIVEN APPLICATION MODELING FOR SYSTEM-LEVEL PERFORMANCE ANALYSIS
R Marculescu and A Nandi, Carnegie Mellon U, USA

Track B: SystemC-SV - AN EXTENSION OF SystemC FOR MIXED MULTI-LEVEL COMMUNICATION MODELLING AND INTERFACE-BASED SYSTEM DESIGN
R Siegmund and D Mueller, TU Chemnitz, D

Track C: EFFICIENT TEST DATA COMPRESSION AND DECOMPRESSION FOR SYSTEM-ON-A-CHIP USING INTEGRAL SCAN CHAINS AND GOLOMB CODING
A Chandra and K Chakrabarty, Duke U, USA

PLENARY – KEYNOTE SESSION

0915

Blue Room – Level 2

Moderator: J da Franca, ChipIdea, PT

ON NANOSCALE INTEGRATION AND GIGASCALE COMPLEXITY IN THE POST .COM WORLD
Hugo De Man, Professor, KU Leuven, Senior Research Fellow, IMEC, BE

While process technologists are obsessed to follow Moore's curve down to nanoscale dimensions, design technologists are confronted with gigascale complexity. On the other hand, post-PC and post dotcom products require zero cost, zero energy yet software programmable novel system architectures to be sold in huge volumes and to be designed in exponentially decreasing time. How do we cope with these novel silicon architectures? What challenges in research does this create? How to create the necessary tools and skills and how to organise research and education in a world driven by shareholders value? Can you spare half an hour to reflect on these challenges to the design community?

GLOBAL RESPONSIBILITIES IN SoC DESIGN
Taylor Scanlon, President & CEO, Virtual Silicon Technology, US

The technical complexities of advanced SoC design are compounded by changes in the economic structure of the worldwide semiconductor industry. A look at some of the organisational and personal responsibilities that will be required to meet the challenges of SoC design in the Future

1030 BREAK

TYPES OF PAPERS

Tracks A, B, C, D and E of the conference programme will present scientific papers that have been reviewed based on their innovative contribution. These papers are published in the Main Proceedings. Track F contains the Designers' Forum papers describing experiences in design and test from the perspective of the user, the tester and the vendor. These contributions are published in a separate volume, the Designers' Forum Proceedings. Full papers are allocated a 30 minute time slot for presentations and questions. Short papers are allocated a 15 minute time slot for presentation and questions.

In many of the sessions, poster authors will use one slide to briefly introduce their work, before making their presentation in the break immediately following. Posters will be grouped conveniently outside the rooms in which they are briefly introduced.

(S) = Short presentation

1A HOT TOPIC – How to Choose Semiconductor IP?

Room A

Organiser: Yervant Zorian, Virage Logic, US
Moderator: Nic Mokhoff, EE Times, US

The session concentrates on today's multidimensional criteria for Choosing Semiconductor IP, including interoperability, flexibility, optimisation, validation, portability, retargetability, manufacturability and certification. Participants represent the different IP market segments.

1100 EMBEDDED PROCESSORS
I Phillips, ARM, UK

1115 EMBEDDED ANALOGUE CORES
J da Franca, ChipIdea, PT

1130 EMBEDDED MEMORY CORES
V Ratford, Virage Logic, US

1145 EMBEDDED SOFTWARE
G Martin, Cadence, US

1200 STANDARDISATION
L Rosenberg, VSIA, US

1215 METHODOLOGY
P Bricaud, Mentor Graphics, FR

1230 LUNCH

1B Formal Verification of Complex Designs

Room B

Moderators: L Fix, Intel, ISR
T Kropf, Bosch, DE

Hardware designs are becoming more and more complex, i.e. deep pipeline and out-of-order architectures. Formally verifying these advanced designs imposes a special challenge with respect to technology and methodology.

1100 FORMAL VERIFICATION OF THE PENTIUM 4 FLOATING-POINT MULTIPLIER
R Kaivola and N Narasimhan, Intel Corp, US

1130 (S) USING REWRITING RULES AND POSITIVE EQUALITY TO FORMALLY VERIFY WIDE-ISSUE OUT-OF-ORDER MICROPROCESSORS WITH A REORDER BUFFER
M N Velev, Carnegie Mellon U, US

1145 (S) AUTOMATIC VERIFICATION OF IN-ORDER EXECUTION IN MICROPROCESSORS WITH FRAGMENTED PIPELINES AND MULTICYCLE FUNCTIONAL UNITS
P Mishra, N Dutt and A Nicolau, UC Irvine, US
H Tomiyama, ISIT, Fukuoka, JP

1200 A CASE STUDY FOR THE VERIFICATION OF COMPLEX TIMED CIRCUITS: IPCMOS
M A Peña, J Cortadella, E Pastor and A Smirnov, TU Catalonia, ES

1230 POSTERS
1B - 1 AN APPROACH TO MODEL CHECKING FOR NONLINEAR ANALOG SYSTEMS
W Hartong, L Hedrich and E Barke, Hannover U, DE

1235 LUNCH

1C Cooling Layout Arrangements

Room C

Moderators: R H J M Otten, TU Eindhoven, NL
M D F Wong, Texas U, US

Annealing has been a resort for combinatorial optimisation problems for 20 years now. Time for a fresh look at its inspirational source! This will be followed by improvements on its application to floorplanning and packing.

1100 FPGA PLACEMENT BY THERMODYNAMIC COMBINATORIAL OPTIMIZATION
J De Vicente, E.T.S.I.A.N., ES
J Lanchares and R Hermida, Madrid Complutense U, ES

1130 AN ENHANCED Q-SEQUENCE AUGMENTED WITH ESSENTIAL EMPTY ROOM INSERTIONS AND PARENTHESIS TREES
C Zhuang and Y Kajitani, Kitakyushu U, JP
K Sakanushi and L Jin, Tokyo IT, JP

1200 ARBITRARY CONVEX AND CONCAVE RECTILINEAR MODULE PACKING USING TCG
J-M Lin, H-L Chen and Y-W Chang, National Taiwan U, ROC

1230 POSTERS
1C - 1 TRANSFORMING ARBITRARY STRUCTURES INTO TOPOLOGICALLY EQUIVALENT SLICING STRUCTURES
O Peyran and W Zhuang, Singapore Inst. of High Performance Computing, SING

1C - 2 A NEW FORMULATION FOR SOC FLOORPLAN AREA MINIMIZATION PROBLEM
C-H Lee, Y-C Lin, W-Y Fu, C-C Chang and T-M Hsieh, Chung-Yuan Christian U, ROC

1C - 3 NON-RECTANGULAR SHAPING AND SIZING OF SOFT MODULES FOR FLOORPLAN DESIGN IMPROVEMENT
C C N Chu, F Y Young and W S Luk, The Chinese U, HK

1235 LUNCH

1D Defect Oriented Test

Room D

Moderators: J Segura, Illes Balears U, ES
H Manhaeve, Q-Star Test, BE

This session deals with the key issues of structural defect based test. The contributions in the session cover defects, their detection, required ATPG, and the application of defect oriented test approaches.

1100 A TEST DESIGN METHOD FOR FLOATING GATE DEFECTS (FGD) IN ANALOG INTEGRATED CIRCUITS
M Pronath, H Graeb and K Antreich, TU Munich, DE

1130 EXACT GRADING OF MULTIPLE PATH DELAY FAULTS
S Padmanaban and S Tragoudas, Southern Illinois U, US

1200 (S) MODELING TECHNIQUES AND TESTS FOR PARTIAL FAULTS IN MEMORY DEVICES
A Al-Ars and A J van de Goor, TU Delft, NL

1215 (S) A NEW ATPG ALGORITHM TO LIMIT TEST SET SIZE AND ACHIEVE MULTIPLE DETECTIONS OF ALL FAULTS
S Lee, B Cobb, J Dworak and M R Mercer, Texas A&M U, US

1230 POSTERS

1D - 1 FINDING A COMMON FAULT RESPONSE FOR DIAGNOSIS DURING SILICON DEBUG
I Pomeranz, Purdue U, US
J Rajski, Mentor Graphics, US
S M Reddy, Iowa U, US

1D - 2 IDDT TESTING OF EMBEDDED CMOS SRAMs
S A Kumar, R Z Makki and D Binkley, North Carolina U, Charlotte, US

1D - 3 FAULT DETECTION AND DIAGNOSIS USING WAVELET BASED TRANSIENT CURRENT ANALYSIS
S Bhunia and K Roy, Purdue U, US

1235 LUNCH

1E Power Analysis and Management in Networks and Processors

Room E

Moderators: E Macii, Politecnico di Torino, IT
K Roy, Purdue U, US

This session presents topics on power consumption analysis of processors and of networks of processors, as well as power management techniques for such systems.

1100 ENERGY EFFICIENT NOISE TOLERANCE FOR ON-CHIP DATA BUSES
D Bertozzi and L Benini, Bologna U, IT
G De Micheli, Stanford U, US

1130 MANAGING POWER CONSUMPTION IN NETWORKS ON CHIPS
T Simunic, HP Labs, USA

1200 (S) COMPETITIVE ANALYSIS OF DYNAMIC POWER MANAGEMENT STRATEGIES FOR SYSTEMS WITH MULTIPLE POWER SAVINGS STATES
S Irani, R Gupta and S Shukla, UC Irvine, US

1215 (S) AccuPower: AN ACCURATE POWER ESTIMATION TOOL FOR SUPERSCALAR MICROPROCESSORS
D Ponomarev, G Kucuk and K Ghose, NY State U, US

1230 POSTERS

1E - 1 POWER MODELING AND REDUCTION OF VLIW PROCESSORS
W Liao and L He, Wisconsin U, Madison, US

1E - 2 AN INSTRUCTION-LEVEL METHODOLOGY FOR POWER ESTIMATION AND OPTIMIZATION OF EMBEDDED VLIW CORES
A Bona, M Sami, D Sciuto and V Zaccaria, Politecnico di Milano, IT
C Silvano, Milano U, IT
R Zafalon, STMicroelectronics

1235 LUNCH

1F System Specifications and Design Flows (Designers' Forum)

Room F

Moderator: V Gerousis, Infineon, DE

This session addresses system specification at high-levels of abstraction, considering in particular SystemC as specification language. A SystemC based design flow is also evaluated. Finally hardware and software co-design methodologies are presented.

1100 (S) EFFICIENT DESIGN FLOW FROM SYSTEM LEVEL TO HARDWARE IN COCENTRIC SYSTEM STUDIO
H Dawid, S Thiel, H Elders-Boll, M Vaupel, E Geesmann, M Vellachi and M Antweiler, Synopsys, IND

1115 (S) SystemC PERFORMANCE EVALUATION USING A PIPELINED DLX MULTIPROCESSOR
C Charest and E M Aboulhamid, Montreal U, CA
C Pilkington and P Paulin, STMicroelectronics, FR

1130 (S) SystemC SPECIFICATION OF A TELECOM PCI-COMPATIBLE INTERFACE
M Bombana, Siemens ICN, IT
F Bruschi, F Ferrandi and D Sciuto, Politecnico di Milano, IT

1145 (S) TRANSACTION LEVEL MODELING OF SoC PLATFORMS USING SystemC
R Hilderink and S Klostermann, Synopsys, DE

1200 (S) TOWARDS BRIDGING THE PRECISION GAP BETWEEN SoC TRANSACTIONAL AND CYCLE-ACCURATE LEVELS
A Clouard, G Mastrorocco, F Carbognani and F Ghenassia, STMicroelectronics, FR

1215 (S) HARDWARE AND SOFTWARE CODESIGN WITH USING SystemC AND BACH
Y Yuyama, K Takai, K Kobayashi and H Onodera, Kyoto U, JP

1230 LUNCH

1G CTO PANEL

Room G

1330-1500
Organiser: L Eberle, EDA Consortium, US

Moderator: C Edwards, EE Times, US

Panellists: W Rhines, Mentor Graphics, US
R Camposano, Synopsys, US
T Vucurevich, Cadence, US
F Neppl, Infineon, DE

Although electronic design automation (EDA) has played an increasingly critical role in the design of semiconductors for over three decades, a plethora of potential challenges face both the EDA industry and their customers who rely on them. Where will design technology be in 3 to 5 years? Will it become a 7 billion industry by 2005? In this panel, chief specialists from the three major EDA companies and major users of their tools debate these challenges and what they mean for their respective futures.

2A PANEL – What is the Right IP Business Model?

Room A

1500-1630
Organiser: Y Zorian, Virage Logic, US

Moderator: K Bartleson, Synopsys, US

Panellists: J Tully, Gartner Dataquest, US
G Toomajanian, Dain Rauscher Wessels, US
E Desai, Desaisive Technology Research, US
M Hosseini, WIT Soundview, US
V P Essi, AH&H, UA

For the last several years, semiconductor IP has been supplied by over 175 third party IP providers. Numerous business models have been experimented during this period, with different ratios of licensing (EDA-like) and royalty (discrete components) components. Several prominent analysts will forecast the future of IP market and discuss the right IP business models to make this sector viable.

1630 BREAK

2B SAT and BDD Techniques

Room B

Moderators: T Shiple, Synopsys, FR
R Drechsler, Bremen U, DE

Boolean methods are at the core of formal methods. The first paper presents a unification of earlier work on SAT, and successfully applies this theory. The second continues the recent phenomenon of significant tool advances in SAT. The third paper improves upon image computation with BDDs.

1500 USING PROBLEM SYMMETRY IN SEARCH BASED SATISFIABILITY ALGORITHMS
E Goldberg, Cadence Berkeley Labs, US
M R Prasad, Fujitsu Labs of America, US
R K Brayton, UC Berkeley, US

1530 BerkMin: A FAST AND ROBUST SAT-SOLVER
E Goldberg, Cadence Berkeley Labs, US
Y Novikov, Inst. of Eng. Cybernetics of NASB Belarus, BL

1600 DYNAMIC SCHEDULING AND CLUSTERING IN SYMBOLIC IMAGE COMPUTATION
G Cabodi, P Camurati and S Quer, Politecnico di Torino, IT

1630 POSTERS
2B - 1 SPEEDING UP SAT FOR EDA
S Pilarski and G Hu, Synopsys, US

2B - 2 SEARCH-BASED SAT USING ZERO-SUPPRESSED BDDS
F A Aloul, M N Mneimneh and K A Sakallah, Michigan U, US

1635 BREAK

2C Technology and Interconnect Issues in Low Power Design

Room C

Moderators: S Huss, TU Darmstadt, DE
D Auvergne, LIRMM, F

This session is concerned with power saving solutions through crosstalk reduction, dynamic voltage scaling, and power/ground mesh sizing.

1500 WIRE PLACEMENT FOR CROSSTALK ENERGY MINIMIZATION IN ADDRESS BUSES
L Macchiarulo, E Macii and M Poncino, Politecnico di Torino, IT

1530 DYNAMIC Vth SCALING SCHEME FOR ACTIVE LEAKAGE POWER REDUCTION
C H Kim and K Roy, Purdue U, US

1600 (S) PROFILE-BASED DYNAMIC VOLTAGE SCALING USING PROGRAM CHECKPOINTS
A Azevedo, I Issenin, R Cornea, R Gupta, N Dutt, A Veidenbaum and A Nicolau, UC Irvine, US

1615 (S) SIZING POWER/GROUND MESHES FOR CLOCKING AND COMPUTING CIRCUIT COMPONENTS
A Mukherjee, K Wang and M Marek-Sadowska, UC Santa Barbara, US

1630 POSTERS

2C - 1 EZ ENCODING: A CLASS OF IRREDUNDANT LOW POWER CODES FOR DATA ADDRESS AND MULTIPLEXED ADDRESS BUSES
Y Aghaghiri and M Pedram, Southern California U, US
F Fallah, Fujitsu Labs of America, US

2C - 2 ESTIMATION OF POWER CONSUMPTION IN ENCODED DATA BUSSES
A Garcia, L D Kabulepa and M Glesner, TU Darmstadt, DE

1635 BREAK

2D Advanced Mixed Signal Test

Room D

Moderators: J L Huertas, CNM-IMSE, ES
B Kaminska, Fluence Technology, US

Enhanced performance test of mixed signal circuits like. RF and analogue IPs, are presented. Several techniques are proposed for the improvement of testability.

1500 A SIGNATURE TEST FRAMEWORK FOR RAPID PRODUCTION TESTING OF RF CIRCUITS
R Voorakaranam, S Cherubal and A Chatterjee, Ardext Technologies, US

1530 PERFORMANCE DRIVEN TEST OF EMBEDDED ANALOG IP
C Guardini, P McNamara, L Daldoss, S Saxena, S Zanella, W Xiang and S Liu, PDF Solutions, US

1600 (S) A NEW DESIGN FLOW AND TESTABILITY MEASURE FOR THE GENERATION OF A STRUCTURAL TEST AND BIST FOR ANALOGUE AND MIXED-SIGNAL CIRCUITS
C Hoffmann, Hannover U, DE

1615 (S) HARD FAULT DETECTION IN MIXED-SIGNAL ICS BY DYNAMIC CURRENT TEST
Y Lechuga, R Mozuelos, M Martinez and S Bracho, Cantabria U, ES

1630 POSTERS

2D - 1 AN EFFICIENT TEST AND DIAGNOSIS SCHEME FOR THE FEEDBACK TYPE OF ANALOG CIRCUITS WITH MINIMAL ADDED CIRCUITS
J W Lin and C L Lee, National Chiao Tung U, ROC
J-E Chen, Chung Hwa U, ROC

2D - 2 ON THE USE OF AN OSCILLATION-BASED TEST METHODOLOGY FOR CMOS MICRO-ELECTRO-MECHANICAL SYSTEMS
V Beroulle, Y Bertrand, L Latorre and P Nouet, LIRMM, FR

1635 BREAK

2E Collaborative Design – Web-Services, Infrastructure, Applications

Room E

Moderators: A Sauer, FhG EAS/IIS, DE
A Pawlak, ITE Warsaw, PL

Collaborative design is an emerging way of designing complex systems in a distributed fashion. The four papers and two posters of this session cover various aspects of this field: distributed catalogues for IP-based design, usage of collaborative work for test generation, existing and visionary framework technologies for collaborative electronic systems design. Additional aspects covered include e-learning and repository technology.

1500 (S) E-DESIGN BASED ON THE REUSE PARADIGM
A Dziri, L Ghanmi, A Ghrab, M Hamdoun, B Missaoui and K Skiba, CSI/INPG, FR
G Saucier, Design & Reuse, FR
M Zrigui, Faculté des Sciences Monastir, TN

1515 INTERNET-BASED COLLABORATIVE TEST GENERATION WITH MOSCITO
A Schneider and K-H Diener, FhG (IIS/EAS), DE
E Ivask, J Raik and R Ubar, TU Tallinn, EST
P Miklos, T Cibakova and E Gramatova, Inst. for Informatics (IIN), SLK

1545 A TWO-TIER DISTRIBUTED ELECTRONIC DESIGN FRAMEWORK
T Kazmierski and N Clayton, Southampton U, UK

1615 (S) EMBEDDED SYSTEM DESIGN BASED ON WEBSERVICES
A Rettberg, Paderborn U/G-LAB, DE
W Thronicke, Siemens/C-LAB, DE

1630 POSTERS

2E - 1 THE FRAUNHOFER KNOWLEDGE NETWORK (FKN) FOR TRAINING IN CRITICAL DESIGN DISCIPLINES
A Sauer and G Elst, FhG IIS/EAS, DE
L Krahn and W John, FhG IZM, DE

2E - 2 COMPARATIVE ANALYSIS AND APPLICATION OF DATA REPOSITORY INFRASTRUCTURE FOR COLLABORATION-ENABLED DISTRIBUTED DESIGN ENVIRONMENTS
L S Indrusiak, TU Darmstadt, DE/UFRGS, BRZ
M Glesner, TU Darmstadt, DE
R Reis, UFRGS, BRZ

1635 BREAK

2F PANEL – Who Owns the Platform?

Room F

1500-1630
Organiser/ Moderator: W Wolf, Princeton U, US
Panellists: M Pinto, Agere, US
P Paulin, STMicroelectronics, CA
C Rowen, Tensilica, US
O Levia, Improv, US
G Saucier, Design & Reuse, FR
V Gerousis, Infineon, DE

As VLSI technology advances, it forces changes in the business organisation of the industry. Traditional vertically integrated semiconductor manufacturers are concentrating less on manufacturing and more on providing novel platforms for important applications. In the middle, fabless semiconductor companies try to create new and improved platforms as well. At the other end, IP companies provide platforms without themselves designing chips.

This poses technical and business challenges:
- Who will develop the platforms? IP houses, fabless semi companies, traditional companies?
- Will customers dictate platforms to semiconductor houses or will the semiconductor houses dictate product categories to the systems houses?
- How do IP firms and fabless semiconductor houses divide up the work and the profits?

1630 BREAK

3A EMBEDDED TUTORIAL – The Need for Infrastructure IP in SoCs

Room A

1700-1830
Organiser: D Gizopoulos, Piraeus U, GR

Moderator: G Smith, Gartner Dataquest, US

Speakers: M Milligan, HPL Technologies, US
Y Zorian, Virage Logic, US
S Pateras, LogicVision, US
M Nicolaidis, iRoC Technologies, FR

With each new generation of semiconductor technology, the manufacturing process is becoming finer and denser, hence resulting in chips more susceptible to defectivity. Today's very deep submicron semiconductor technologies of 0.13u and below have reached susceptibility levels that put semiconductor reliability, diagnosis and yield at risk, if they were based on conventional processes.

This Embedded Tutorial discusses the key trends impacting manufacturing yield and field reliability and covering the above challenges of increased susceptibility. The set of presentations will describe the range of infrastructure IP solutions from embedded diagnosis, and embedded error tolerance, to embedded repair.

1830 CLOSE

3B Advances in Logic Synthesis

Room B

Moderators: M Berkelaar, Magma Design Automation, NL
W Kunz, Kaiserslautern U, DE

The papers in this session explore less beaten paths in logic synthesis. The first one proposes a heuristic algorithm for static reduction not based on enumeration of compatibles. The second one describes a method to derive self-timed circuits from synchronous ones and the last one modifies domino logic to improve performance under noise and power considerations.

1700 CHESMIN: A HEURISTIC ALGORITHM FOR STATE REDUCTION IN INCOMPLETELY SPECIFIED FINITE STATE MACHINES
S Goren, PMC-Sierra, US
F J Ferguson, UC Santa Barbara, US

1730 GENERALIZED EARLY EVALUATION IN SELF-TIMED CIRCUITS
M A Thornton, K Fazel and R B Reese, Mississippi State U, US
C Traver, Union College, US

1800 DUAL THRESHOLD VOLTAGE DOMINO LOGIC SYNTHESIS FOR HIGH PERFORMANCE WITH NOISE AND POWER CONSTRAINT
S-O Jung, Illinois Urbana-Champaign U, US
K-W Kim, Pluris Inc, US
S-M Kang, UC Santa Cruz, US

1830 POSTERS

3B - 1 AN ENCODING TECHNIQUE FOR LOW POWER CMOS IMPLEMENTATIONS OF CONTROLLERS
M Martinez, M J Avedillo, J M Quintana, M Koegst, S T Ruelke and H Susse, CNM-IMSE, ES

3B - 2 COMPOSITION TREES IN FINDING BEST VARIABLE ORDERINGS FOR ROBDDs
E Dubrova, Royal IT, SE

3B - 3 A DIRECT MAPPING SYSTEM FOR DATAPATH MODULE AND FSM IMPLEMENTATION INTO LUT-BASED FPGAs
J Abke and E Barke, Hannover U, DE

3B - 4 CONCURRENT AND SELECTIVE LOGIC EXTRACTION WITH TIMING CONSIDERATION
P Rezvani and M Pedram, Southern California U, US

3B - 5 IMPROVED TECHNOLOGY MAPPING FOR PAL-BASED DEVICES USING A NEW APPROACH TO MULTI-OUTPUT BOOLEAN FUNCTIONS
K Dariusz, Silesian UT, PL

3B - 6 EFFICIENT AND EFFECTIVE REDUNDANCY REMOVAL FOR MILLION-GATE CIRCUITS
M Berkelaar and K van Eijk, Magma Design Automation, NL

1835 CLOSE

3C Novel Applications of Symbolic Techniques to Analogue and Digital Circuit Design

Room C

Moderators: F V Férnandez, IMSE-CNM, ES
A Konczykowska, Alcatel R&I, FR

The three first papers of this session present new applications of symbolic analysis to analogue circuit design, with a special emphasis on nonlinear circuit characteristic. The proposed approaches open new vistas on circuit synthesis and behavioural modelling. The last paper proposes a new symbolic decomposition technique based on Taylor expansion for the formal verification of digital circuits.

1700 A FITTING APPROACH TO GENERATE SYMBOLIC EXPRESSIONS FOR LINEAR AND NONLINEAR PERFORMANCE CHARACTERISTICS
W Daems, G Gielen and W Sansen, KU Leuven, BE

1730 (S) PARAMETER CONTROLLED AUTOMATIC SYMBOLIC ANALYSIS OF NONLINEAR ANALOG CIRCUITS
R Popp, J Oehmen, L Hedrich and E Barke, Hannover U, DE

1745 (S) CONSTRUCTING SYMBOLIC MODELS FOR THE INPUT/OUTPUT BEHAVIOUR OF PERIODICALLY TIME-VARYING SYSTEMS USING HARMONIC TRANSFER MATRICES
P Vanassche, G Gielen and W Sansen, KU Leuven, BE

1800 TAYLOR EXPANSION DIAGRAMS: A COMPACT, CANONICAL REPRESENTATION WITH APPLICATIONS TO SYMBOLIC VERIFICATION
M Ciesielski, P Kalla and Z Zeng, U Massachusetts Amherst, US
B Rouzeyre, LIRMM, FR

1830 POSTERS

3C - 1 OPTIMIZATION TECHNIQUES FOR DESIGN OF GENERAL AND FEEDBACK LINEAR ANALOG AMPLIFIER WITH SYMBOLIC ANALYSIS
T C Hieu and E-H Horneber, TU Braunschweig, DE

3C - 2 CRITICAL COMPARISON AMONG SOME ANALOG FAULT DIAGNOSIS PROCEDURES BASED ON SYMBOLIC TECHNIQUES
A Luchetta, Basilicata C. da Macchia U, IT
S Manetti and M C Piccirilli, Florence U, IT

1835 CLOSE

3D HOT TOPIC – EDA Tools for RF: Myth or Reality?

Room D

Organisers: L Guarnirei, Barcelona Design, US
E Chen, Celestry Design Technologies, US

Moderators: H Reiter, Barcelona Design, US
C Ajluni, Celestry Design Technologies, US

Designing circuits that operate at radio frequencies (above 1 GHz) is a challenge for many reasons. Nearly every aspect of producing chips is stressed at high frequency, including technology development, modelling, CAD, design, integration, and packaging. This session will debate the pros and cons of RF CMOS design and related modelling. Will, for example, access to tools for accurate RF simulation convince the nay sayers of the viability of RF CMOS design? And, if so, what will it take to achieve this accuracy?

1700 SIMULATION CHALLENGES FACING THE RFIC INDUSTRY
S Savage, Modeling Group Leader, Cypress Semiconductors, US

1730 EDA TOOLS FOR RF: MYTH OR REALITY?
M Hershenson, Chief Technology Officer, Barcelona Design, US

1800 RF CMOS DESIGN– BIG ISSUES, BIG REWARDS
X Zhang, VP of R&D, Device Modeling, Celestry Design Technologies, US

1830 CLOSE

3E Platform-Based Design and Virtual-Component Reuse

Room E

Moderators: W Wolf, Princeton U, US
N Mártinez Madrid, FZI Karlsruhe, DE

This session presents new algorithms, techniques and methodologies for virtual-component reuse and platform-based design dedicated to digital and mixed-signal systems. First, a paper discussing a dynamic runtime re-scheduling algorithm for platform-based design is presented. Afterwards, a technique for describing virtual components in a high-level language is introduced. Finally, a design reuse methodology for mixed-signal systems is demonstrated.

1700 DYNAMIC RUNTIME RE-SCHEDULING ALLOWING MULTIPLE IMPLEMENTATIONS OF A TASK FOR PLATFORM-BASED DESIGNS
T M Lee and W Wolf, Princeton U, US
J Henkel, NEC, US

1730 TECHNIQUES TO EVOLVE A C++ BASED SYSTEM DESIGN LANGUAGE
R Pasko and S Vernalde, IMEC, BE
P Schaumont, UC Los Angeles, US

1800 A MIXED-SIGNAL DESIGN REUSE METHODOLOGY BASED ON PARAMETRIC BEHAVIOURAL MODELS WITH NON-IDEAL EFFECTS
A J Gines and E Peralias, IMSE-CNM, ES
N Martinez Madrid and R Seepold, FZI Karlsruhe, DE

1830 POSTERS
3E - 1 AREA-EFFICIENT MEMORY FOR SELF-PROFILING MICROPROCESSOR PLATFORMS
S Cotterell, F Vahid and R Lysecky, UC Riverside, US

3E - 2 FlexBench: REUSE OF VERIFICATION IP TO INCREASE PRODUCTIVITY
S Stoehr, M Simmons and J Geishauser, Motorola Munich, DE

1835 CLOSE

3F1 Security and IP Issues in Design Flows (Designers' Forum)

Room F

Moderator: E M Aboulhamid, Montreal U, CA

This session will present two case studies for security components and then two papers introducing two different design flows that consider IP management.

1700 (S) DESIGN OF SECURE ENCRYPTION IN DSP EMBEDDED PROCESSORS
C Gebotys, Waterloo U, CA

1715 (S) EVALUATING DESIGN ALTERNATIVES FOR EFFICIENT PUBLIC-KEY SECURITY PROCESSING ON WIRELESS HANDSETS
N Potlapally, S Ravi and A Raghunathan, NEC, US
G Lakshminarayana, Alphion Corp., US

1730 (S) INTEGRATING IP INTO TODAY'S SoC DESIGN FLOWS
T Daniels, LSI Logic, UK

1745 (S) IP REUSE: NEXT SoC REUSE OR PATCHWORK
P Bricaud and T Delaye, Mentor Graphics, FR
M Eftimakis, NewLogic, US

3F2 Analogue Circuit Characterisation and Simulation

Room F

Moderators: A Ródriguez-Vázquez, IMSE-CNM, ES
D Leenaerts, Philips, NL

This session combines two papers from the field of analogue characterisation and simulation, namely characterisation of a bipolar transistor and simulation of oscillators.

1800 TEST STRUCTURE FOR Ic(Vbe) PARAMETER DETERMINATION OF LOW VOLTAGE ALGORITHMS
W Rahajandraibe, C Dufaza and D Auvergne, LIRMM, FR
B Cialdella, B Majoux and V Chowdhury, STMicroelectronics, FR

1830 (S) GLOBAL OPTIMIZATION APPLIED TO THE OSCILLATOR PROBLEM
S Lampe and S Laur, Bremen U, DE

1845 POSTERS
3F2 - 1 STEADY STATE CALCULATION OF OSCILLATORS USING CONTINUATION METHODS
H G Brachtendorf, S Lampe and R Laur, Bremen U, DE
R Melville, Agere Systems, US
P Feldmann, Celight Inc, US

1850 CLOSE

WEDNESDAY 6 MARCH, 2002

4A PANEL – MEDEA+ and ITRS Roadmaps

Room A

0900-1030
Organiser: W Rosenstiel, FZI/Tuebingen U, DE

Moderator G Mathéron, Director of MEDEA+ Office, FR

Panellists: A A Jerraya, TIMA, Grenoble, FR
W Joyner, IBM, US
M Rogers, Intel, US
W Rosenstiel, FZI/Tuebingen U, DE
I Rugen-Herzig, Infineon Technologies, DE
F Theeuwen, Philips Research, NL

The panellists will present the strategies in their respective fields of interest, resulting from their working groups conclusions. They will underline the breakthroughs and potential developments of solutions and the milestones to reduce design times and increase design quality. The focus will be on application driven solutions, mostly in the SoC domains (covering both hardware, embedded and application softwares).

1030 BREAK AND POSTER SESSION

4B Asynchronous Circuits and Clock Scheduling

Room B

Moderators: M Renaudin, TIMA, Grenoble, FR
L Lavagno, Politecnico di Torino, IT

This session includes three papers presenting different techniques to solve problems related to the synthesis of asynchronous circuits and the verification of clock schedules. The first paper presents a complete framework for the synthesis of asynchronous circuits from a CSP-like language. The second paper proposes a new method to detect state coding conflicts in asynchronous specifications. The third paper presents a polynomial time algorithm to verify clock schedules in the presence of cross talk.

0900 A BURST-MODE ORIENTED BACK-END FOR THE BALSA SYNTHESIS SYSTEM
T Chelcea and S M Nowick, Columbia U, US
A Bardsley and D Edwards, Manchester U, UK

0930 DETECTING STATE CODING CONFLICTS IN STGs USING INTEGER PROGRAMMING
V Kohmenko, M Koutny and A Yakovlev, Newcastle upon Tyne U, UK

1000 VERIFYING CLOCK SCHEDULES IN THE PRESENCE OF CROSS TALK
S Hassoun, E H Calvillo-Gamez and C Cromer, Tufts U, US

1030 POSTERS

4B - 1 VISUALIZATION OF PARTIAL ORDER MODELS IN VLSI DESIGN FLOW
A Bystrov, M Koutny and A Yakovlev, Newcastle upon Tyne U, UK

4B - 2 HIGH-LEVEL MODELING AND DESIGN OF ASYNCHRONOUS ARBITERS FOR ON-CHIP COMMUNICATION SYSTEMS
J-B Rigaud, L Fesquet and M Renaudin, TIMA, Grenoble, FR
J Quartana, STMicroelectronics, FR

1035 BREAK AND POSTER SESSION

4C Analogue and Mixed-Signal Systems

Room C

Moderators: A Kaiser, ISEN, FR
P Wambacq, IMEC, BE

This session covers both analogue and mixed-signal systems and subsystems. It addresses some hot topic items in this field, namely RF, high-speed data converters and vision systems -on-chip.

0900 ANALYSIS OF NONLINEARITIES IN RF FRONT-END ARCHITECTURES USING A MODIFIED VOLTERRA SERIES APPROACH
M Goffioul, P Wambacq, G Vandersteen and S Donnay, IMEC, BE

0930 SYSTEMATIC DESIGN OF A 200 MS/s 8BIT INTERPOLATING A/D CONVERTER
J Vandenbussche, E Lauwers, K Uyttenhove, M Steyaert and G Gielen, KU Leuven, BE

1000 BIO-INSPIRED ANALOG VLSI DESIGN REALIZES PROGRAMMABLE COMPLEX SPATIO-TEMPORAL DYNAMICS ON A SINGLE CHIP
R Carmona, F Jimenez-Garrido, R Dominguez-Castro, S Espejo and A Rodriguez-Vazquez, IMSE-CNM, ES

1030 POSTERS

4C - 1 THE SELECTIVE PULL-UP (SP) NOISE IMMUNITY SCHEME FOR DYNAMIC CIRCUITS
M R Stan and A Panigrahi, Virginia U, US

4C - 2 DESIGN AND VALIDATION FLOW INCLUDING SUBSTRATE PARASITIC EXTRACTION FOR RF CIRCUITS
A Cathelin, D Saias and D Belot, STMicroelectronics, FR
Y Leclercq and F Clement, Simplex Solutions, FR

4C - 3 A COMPLETE PHASE-LOCKED LOOP POWER CONSUMPTION MODEL
D Duarte, V Narayanan and M J Irwin, The Pennsylvania State U, US

1035 BREAK AND POSTER SESSION

4D BIST Diagnosis and DFT

Room D

Moderators: M-L Flottes, LIRMM, FR
A Benso, Politecnico di Torino, IT

This session discusses several novel techniques to optimise test application time, diagnosability and test coverage of complex random logic blocks.

0900 (S) AN INCREMENTAL ALGORITHM FOR TEST GENERATION IN ILLINOIS SCAN-ARCHITECTURE BASED DESIGNS
A R Pandey and J H Patel, Illinois U, Urbana-Champaign, US

0915 (S) GATE LEVEL FAULT DIAGNOSIS IN SCAN-BASED BIST
I Bayraktaroglu and A Orailoglu, UC San Diego, US

0930 AN INTERVAL-BASED DIAGNOSIS SCHEME FOR IDENTIFYING FAILING VECTORS IN A SCAN-BIST ENVIRONMENT
C Liu and K Chakrabarty, Duke U, US
M Goessel, Potsdam U, DE

1000 REDUCING TEST APPLICATION TIME THROUGH TEST DATA MUTATION ENCODING
S Reda and A Orailoglu, UC San Diego, US

1030 POSTERS
4D - 1 DIRECTED-BINARY SEARCH IN LOGIC BIST DIAGNOSTICS
R Kapur and T W Williams, Synopsys, US
M R Mercer, Texas A&M U, US

4D - 2 AN EVOLUTIONARY APPROACH TO THE DESIGN OF ON-CHIP PSEUDORANDOM TEST GENERATORS
M Favalli, DI- Ferrara U, IT
M Dalpasso, DEI – Padova U, IT

1035 BREAK AND POSTER SESSION

4E Code and Memory Optimisation in Co-Design

Room E

Moderators: R Leupers, TU Aachen, DE
R Ernst, TU Braunschweig, DE

This session focusses on code generation issues in embedded system design. The first paper deals with processor customisation for turbo code applications. The second paper presents an efficient technique for exploiting reduced bitwidth instruction set architectures. The last paper utilises scratch pad memory for energy reduction of embedded software.

0900 HARDWARE/SOFTWARE TRADE-OFFS FOR ADVANCED 3G CHANNEL CODING
H Michel, A Worm and N Wehn, Kaiserslautern U, DE
M Muench, Alcatel, BE

0930 AN EFFICIENT COMPILER TECHNIQUE FOR CODE SIZE REDUCTION USING REDUCED BIT-WIDTH ISAs
A Halambi, A Shrivastava, P Biswas, N Dutt and A Nicolau, UC Irvine, US

1000 ASSIGNING PROGRAM AND DATA OBJECTS TO SCRATCHPAD FOR ENERGY REDUCTION
S Steinke, L Wehmeyer, B-S Lee and P Marwedel, Dortmund U, DE

1030 BREAK AND POSTER SESSION

4F System Design Methodologies (Designers' Forum)

Room F

Moderator: M Bombana, Siemens ICN, IT

This session is devoted to the presentation of different system design methodologies for HW and SW embedded systems.

0900 (S) ADVANCED METHODS FOR SoC CONCURRENT ENGINEERING
F Ghenassia, STMicroelectronics, FR
A Gonier, Mentor Graphics, FR
0915 (S) STANDARD CO-EMULATION API – A FOUNDATION FOR PRODUCTIVE, EMULATION-BASED VERIFICATION SOLUTIONS
R Howarth, IKOS Systems, UK

0930 (S) AN INTEGRATED HETEROGENEOUS SIMULATION ENVIRONMENT ENABLING EFFECTIVE EMBEDDED SOFTWARE DEVELOPMENT
M Thanner, M Rohleder, M Brenner, S Lenk and C Roettgermann, Motorola GmbH, DE

0945 (S) AN EFFICIENT SIMULATION ENVIRONMENT FOR THE DESIGN OF NETWORKED BLUETOOTH DEVICES
Y Ahn, D Kim, S Lee, S Park, S Yoo, K Choi and S-I Chae, Seoul National U, KR

1000 (S) CONTEXT SWITCHING IN A HARDWARE/SOFTWARE CO-DESIGN OF THE JAVA VIRTUAL MACHINE
K B Kent and M Serra, Victoria U, CA

1015 (S) HW/SW CO-DESIGN OF A MULTIPLE INJECTION DRIVER AUTOMOTIVE SUBSYSTEM USING A CONFIGURABLE SYSTEM-ON-CHIP
M Baleani, Ancona U/PARADES EEIG, IT
M Conti, Ancona U, IT
A Ferrari, PARADES EEIG, IT
A Sangiovanni-Vincentelli, UC Berkeley, US/PARADES EEIG, IT

1030 BREAK AND POSTER SESSION

5A HOT TOPIC – Network on a Chip

Room A

Moderator/ Organiser: G De Micheli, Stanford U, US

Systems on chips designed with 50-100nm silicon technologies can exploit networking techniques to implement reliable, noise-tolerant on-chip communication schemes. This session reviews the distinguishing features and challenges of on-chip networking architectures and protocols, and presents industrial prototypes using on-chip network technology.

1100 NETWORKS ON CHIPS: A NEW PARADIGM FOR SYSTEM ON CHIP DESIGN
G De Micheli and L Benini, Stanford U, US

1130 DAYTONA – A COMMUNICATION FABRIC FOR MULTIPROCESSING SYSTEMS ON A CHIP
J Williams, N Heintze and B Ackland, Agere Systems, US

1200 NETWORKS ON SILICON: THE NEXT DESIGN PARADIGM FOR SYSTEMS ON SILICON
K Goossens, E Rijpkema, P Wielage, A Peeters and J van Meerbergen, Philips Research, NL

1230 LUNCH

5B Low Power Architectures and Software

Room B

Moderators: W Nebel, OFFIS, DE
M Miranda, IMEC, BE

This session covers new research contributions for reducing power consumption by exploiting SW-transformations and/or novel architectural extensions for memories.

1100 DATA REUSE EXPLORATION METHODOLOGY FOR LOOP-DOMINATED APPLICATIONS
T Van Achteren, KU Leuven, BE
F Catthoor and R Lauwereins, IMEC, BE

1130 EAC: A COMPILER FRAMEWORK FOR HIGH-LEVEL ENERGY ESTIMATION AND OPTIMIZATION
I Kadayif, M Kandemir, N Vijaykrishnan, M J Irwin and A Sivasubramaniam, Pennsylvania State U, US

1200 (S) POWER SAVINGS IN EMBEDDED PROCESSORS THROUGH DECODE FILER CACHE
W Tang, R Gupta and A Nicolau, UC Irvine, US

1215 (S) HARDWARE-ASSISTED DATA COMPRESSION FOR ENERGY MINIMIZATION IN SYSTEMS WITH EMBEDDED PROCESSORS
L Benini and D Bruni, Bologna U, IT
A Macii and E Macii, Politecnico di Torino, IT

1230 POSTERS

5B - 1 POWER-EFFICIENT TRACE CACHES
J Hu, N Vijaykrishnan, M Kandemir and M J Irwin, Pennsylvania State U, US

5B - 2 TIME DOMAIN MODELING OF THE POWER CONSUMPTION OF A 32 BIT MICROPROCESSOR
G Caldentey, J Cid, J Rius, X Amela, S Manich and R Rodriguez, Catalunya UP, ES

5B - 3 REDUCING CACHE ACCESS ENERGY IN ARRAY-INTENSIVE APPLICATIONS
M Kandemir, Pennsylvania State U, US
I Kolcu, Manchester U, UK

1235 LUNCH

5C Nitty Gritty Details of Layout Design

Room C

Moderators: E Barke, Hannover U, DE
P Groeneveld, Magma Design Automation, NL

The session covers three different parasitic layout problems. The first paper describes an efficient analytical crosstalk model, which is used to evaluate noise avoidance techniques like driver and wire sizing. The second one addresses electromigration and presents a FEM based method to examine expected current densities in metallization patterns. The last paper presents a polynomial time diode insertion and routing algorithm to avoid antenna problems.

1100 ANALYSIS OF NOISE AVOIDANCE TECHNIQUES IN DSM INTERCONNECTS USING A COMPLETE CROSSTALK NOISE MODEL
M Becer and V Zolotov, Motorola Inc, US
D Blaauw, Michigan U, Ann Arbor, US
I Hajj, Illinois U, Urbana-Champaign, US

1130 HIERARCHICAL CURRENT DENSITY VERIFICATION FOR ELECTROMIGRATION ANALYSIS IN ARBITRARY SHAPED METALLIZATION PATTERNS OF ANALOG CIRCUITS
G Jerke and J Lienig, Bosch, DE

1200 A POLYNOMIAL TIME OPTIMAL DIODE INSERTION/ROUTING ALGORITHM FOR FIXING ANTENNA PROBLEM
L-D Huang, X Tang, H Xiang and D F Wong, Texas U at Austin, US
I-M Liu, Silicon Perspective Corporation, US

1230 POSTERS
5C - 1 STATISTICAL TIMING DRIVEN PARTITIONING FOR VLSI CIRCUITS
C Ababei and K Bazargan, Minnesota U, US

1235 LUNCH

5D SoC and System Test

Room D

Moderators: Y Zorian, LogicVision, US
D Gizopoulos, Piraeus U, GR

This session presents new test planning methodologies and optimisation techniques for SoC designs testing as well as a framework for the use of modelling languages in embedded systems testing.

1100 TEST PLANNING AND DESIGN SPACE EXPLORATION IN A CORE-BASED ENVIRONMENT
E Cota, L Carro and M Lubaszewski, UFRGS, BR
A Orailoglu, UC San Diego, US

1130 A HIERARCHICAL TEST SCHEME FOR SYSTEM-ON-CHIP DESIGNS
J-F Li, H-J Huang, J-B Chen, C-P Su and C-W Wu, National Tsing Hua U, ROC
C Cheng, S-I Chen, C-Y Hwang and H-P Ling, Faraday Technology Corp, ROC

1200 (S) EFFICIENT WRAPPER/TAM CO-OPTIMIZATION FOR LARGE SoCs
V Iyengar and K Chakrabarty, Duke U, US
E J Marinissen, Philips, NL

1215 (S) BEYOND UML TO AN END-OF-LINE FUNCTIONAL TEST ENGINE
A Baldini, A Benso, P Prinetto, Politecnico di Torino, IT
S Mo and A Taddei, Magneti Marelli Electronic Systems, IT

1230 POSTERS
5D - 1 FAULT ISOLATION USING TESTS FOR NON-ISOLATED BLOCKS
I Pomeranz, Purdue U, US
Y Zorian, LogicVision, US

1235 LUNCH

5E Modelling and Synthesis of Embedded Systems

Room E

Moderators: J C López, Castilla-La Mancha U, ES
F Rousseau, TIMA, Grenoble, FR

In this session, some issues on system modelling and synthesis are discussed. First, some event model interfaces for system analysis are presented. The second paper deals with a two-step iterative synthesis approach using a DVS processing element. The last two papers are short papers presenting a model of a codesign virtual machine and an automatic method to evaluate the accuracy of fixed point algorithms.

1100 EVENT MODEL INTERFACES FOR HETEROGENEOUS SYSTEM ANALYSIS
K Richter and R Ernst, TU Braunschweig, DE

1130 ENERGY-EFFICIENT MAPPING AND SCHEDULING FOR DVS ENABLED DISTRIBUTED EMBEDDED SYSTEMS
M T Schmitz and B Al-Hashimi, Southampton U, UK
P Eles, Linköping U, SE

1200 (S) A LAYERED, CODESIGN VIRTUAL MACHINE APPROACH TO MODELING COMPUTER SYSTEMS
J M Paul and D E Thomas, Carnegie Mellon U, US

1215 (S) AUTOMATIC EVALUATION OF THE ACCURACY OF FIXED-POINT ALGORITHMS
D Menard and O Sentieys, LASTI – Rennes U, FR

1230 POSTERS
5E - 1 MAPPABILITY ESTIMATION OF ARCHITECTURE AND ALGORITHM
J-P Soininen, J Kreku and Y Qu, VTT Electronics, FI

1235 LUNCH

5F Design Methodologies (Designers' Forum

Room F

Moderator: F Ghenassia, STMicroelectronics, FR

This session addresses different design methodologies issues at the lower levels of abstraction, considering in particular different problems associated with physical design of digital circuits.

1100 (S) A HIERARCHICAL IMPLEMENTATION METHODOLOGY FOR LARGE, COMPLEX, DEEP SUB-MICRON ASICs
K Ewusie, Synopsys, US
N Das and H Bhatnagar, Corrent Corporation, US

1115 (S) A PREDICTIVE AND ANALYTICAL CLOCK PLANNING METHODOLOGY FOR HIERARCHICAL BLOCK BASED DESIGN
R Adhikary, K Venkatramani and S Mantik, Cadence Design Systems, US

1130 (S) FRONT-END PHYSICAL DESIGN SOLUTION PROVIDES HIERARCHICAL METHODOLOGY
V Gerousis, Infineon Technologies, DE
W-J Dai, Silicon Perspective Co, US

1145 (S) USE OF MULTI-PHASE STABILITY INTERVALS TO HANDLE CROSSTALK WITH THE TIMING ANALYSER HiTAS
G Avot, A Greiner and M-M Louerat, UPMC-CNRS/LIP6/ASIM, FR
K Dioury and A Lester, Avertec, FR
A Debreil, Bull, FR

1200 (S) DESIGN AND VALIDATION OF AN ON-CHIP DETECTION CIRCUIT FOR THE VERIFICATION OF IC SUPPLY CONNECTIONS
H Manhaeve and S Kerckenaere, Q-Star Test, BE

1215 (S) SIGNAL INTEGRITY METHODOLOGY ON 300MHz SoC DESIGN USING ALF LIBRARIES AND TOOLS
W Roethig, R Nibhanupudi, A Balakrishnan and G Dandu, NEC Electronics Inc, US
S McCormick, V Srinivas, D Sogani and K Walsh, Sequence Design Inc, US

1230 LUNCH

5G Start-Up CEO Panel

Room G

1330-1500
Organiser/ Moderator: B Courtois, TIMA, Grenoble, FR
Panellists: G Arnout, CoWare, US
E Dupont, iRoC, FR
R Hagelauer, DICE, AT
J-M Karam, Memscap, FR
H Meyr, CADIS, DE

Several CEO's of young companies will share their experiences of starting-up with the attendees.

6A PANEL – Power Crisis in SoC Design: Strategies for Constructing Low-Power, High-Performance SoC Designs

Room A

1500-1630
Organiser: K Brock, Virtual Silicon Technology, US

Moderator: C Edwards, Electronic Times, UK

Panellists: R Lannoo, Alcatel, BE
U Schlichtmann, Infineon Technologies, DE
A Domic, Synopsys, US
J Benkoski, Nanometer Analysis and Test, US
D Overhauser, Interconnect Verification, US
M Kliment, Virtual Silicon, US

With the addition of high-performance features to battery-operated devices and hitting thermal limits in desktop and server devices, automated SoC design methodologies for low power are at a crisis. Traditionally, synthesis tools have focussed on achieving timing closure, routers with area minimisation and floor planners arbitrating between those two often conflicting goals. Dynamic and static power minimisation have been relegated to analysis tools that point out problems designed-in by the construction tools. Algorithm design, device partitioning, power management strategies, low-power circuit design, and low-power silicon processes have been the only fruitful attacks on the problems other than larger batteries and heavy heat sinks. Can EDA and IP help?

This panel will address the current and future EDA tool and design methodology solutions to these problems and examine the solution tradeoffs from various perspectives.

1630 BREAK AND POSTER SESSION

6B Reconfigurable Architectures

Room B

Moderators: R Hartenstein, Kaiserslautern U, DE
U Kebschull, Leipzig U, DE

Motivating the usefulness of run-time reconfiguration, the session starts with a case study of a video comparison algorithm, then follows a top-down approach, thereby covering all levels of abstraction, namely task level, data level and controller level reconfiguration.

1500 A VIDEO COMPRESSION CASE STUDY ON A RECONFIGURABLE VLIW ARCHITECTURE
D Rizzo and O Colavin, STMicroelectronics, US

1530 A COMPLETE DATA SCHEDULER FOR MULTI-CONTEXT RECONFIGURABLE ARCHITECTURES
M Sánchez-Élez, M Férnandez, R Maestre and R Hermida, Madrid Complutense U, ES
N Bagherzadeh and F Kurdahi, UC Irvine, US

1600 (S) HIGHLY SCALABLE DYNAMICALLY RECONFIGURABLE SYSTOLIC RING-ARCHITECTURE FOR DSP APPLICATIONS
G Sassatelli, L Torres, C Diou, G Cambon and J Galy, LIRMM, FR

1615 (S) (SELF-)RECONFIGURABLE FINITE STATE MACHINES: THEORY AND IMPLEMENTATION
J Teich and M Koester, Paderborn U, DE

1630 POSTERS

6B - 1 THE USE OF RUNTIME CONFIGURATION CAPABILITIES FOR NETWORKED EMBEDDED SYSTEMS
C Nitsch and U Kebschull, Leipzig U, DE

6B - 2 A SAT SOLVER USING SOFTWARE AND RECONFIGURABLE HARDWARE
I Skliarova and A B Ferrari, Aveiro U, PT

1635 BREAK AND POSTER SESSION

6C Analogue Modelling, Layout and Sizing

Room C

Moderators: H Graeb, TU Munich, DE
G Gielen, KU Leuven, BE

The session presents new achievements in analogue CAD. The first paper deals with efficient statistical interconnect simulation considering nonlinear devices. The second paper presents a layout generation technique for capacitors with minimum systematic mismatch. The third paper presents an efficient sizing technique that includes process and operational variations. The fourth paper deals with RF amplifier models for system-level simulation. The two posters describe methods for continuous DS modulator simulation and SC circuit sizing.

1500 A LINEAR-CENTRIC SIMULATION FRAMEWORK FOR PARAMETRIC FLUCTUATIONS
E Acar and S Nassif, IBM Austin Research, US
L Pileggi, Carnegie Mellon U, US

1530 AUTOMATIC GENERATION OF COMMON-CENTROID CAPACITOR ARRAYS WITH ARBITRARY CAPACITOR RATE
M Dessouky and D E-D Sayed, ASU, EGY

1600 (S) ANALOG CIRCUIT SIZING USING ADAPTIVE WORST-CASE PARAMETER SETS
R Schwencker, Infineon Technologies/TU Munich, DE
F Schenkel, M Pronath and H Graeb, TU Munich, DE

1615 (S) HIGH-FREQUENCY NONLINEAR AMPLIFIER MODEL FOR THE EFFICIENT EVALUATION OF INBAND DISTORTION UNDER NONLINEAR LOAD-PULL CONDITIONS
G Vandersteen, P Wambacq and S Donnay, IMEC, BE
F Verbeyst, Agilent Technologies, BE

1630 POSTERS

6C – 1 DAISY-CT: A HIGH-LEVEL SIMULATION TOOL FOR CONTINUOUS-TIME DS MODULATORS
K Francken, M Vogels, E Martens and G Gielen, KU Leuven, BE

6C - 2 AUTOMATED OPTIMAL DESIGN OF SWITCHED-CAPACITOR CIRCUITS
A Hassibi and M Hershenson, Barcelona Design, ES

1635 BREAK AND POSTER SESSION

6D Test Resource Partitioning for Embedded Cores

Room D

Moderators: Z Peng, Linköping U, SE
B Rouzeyre, LIRMM, FR

This session deals with several techniques for test resource partitioning and planning, test data compression, and self-checking of core-based systems.

1500 EFFECTIVE SOFTWARE SELF-TEST METHODOLOGY FOR PROCESSOR CORES
N Kranitis and A Paschalis, Athens U, GR
D Gizopoulos, Piraeus U, GR
Y Zorian, LogicVision, US

1530 (S) TEST RESOURCE PARTITIONING AND REDUCED PIN-COUNT TESTING BASED ON TEST DATA COMPRESSION
A Chandra and K Chakrabarty, Duke U, US

1545 (S) IMPROVING COMPRESSION RATIO, AREA OVERHEAD, AND TEST APPLICATION TIME FOR SYSTEM-ON-A-CHIP TEST DATA COMPRESSION/DECOMPRESSION
P T Gonciari and B Al-Hashimi, Southampton U, UK
N Nicolici, McMaster U, CA

1600 PROBLEMS DUE TO OPEN FAULTS IN THE INTERCONNECTIONS OF SELF-CHECKING DATA-PATHS
M Favalli, DI – Ferrara U, IT
C Metra, DEIS – Bologna U, IT

1630 POSTERS
6D - 1 A HEURISTIC FOR TEST SCHEDULING AT SYSTEM LEVEL
M L Flottes, J Pouget and B Rouzeyre, LIRMM, FR

6D – 2 FORMULATION OF SoC TESTING SCHEDULING AS A NETWORK TRANSPORTATION PROBLEM
S Koranne and V Suhas, Philips, NL

1635 BREAK AND POSTER SESSION

6E System Level Simulation and Modelling

Room E

Moderators: B Al-Hashimi, Southampton U, UK
P Schwarz, FhG IIS/EAS Dresden, DE

The session covers different important topics: HW and SW cosimulation, efficient analogue modelling and simulation approaches, and the application of simulation-based energy estimation for low-power asynchronous design.

1500 AUTOMATIC GENERATION OF FAST TIMED SIMULATION MODELS FOR OS IN SoC DESIGN
S Yoo, G Nicolescu, L Gauthier and A A Jerraya, TIMA, Grenoble, FR

1530 WINDOW-BASED SUSCEPTANCE MODELS FOR LARGE-SCALE RLC CIRCUIT ANALYSES
Z Zheng and L Pileggi, Carnegie Mellon U, US
B Krauter, IBM, US

1600 (S) A LINEAR-CENTRIC MODELING APPROACH TO HARMONIC BALANCE ANALYSIS
P Li and L Pileggi, Carnegie Mellon U, US

1615 (S) AN ENERGY ESTIMATION METHOD FOR ASYNCHRONOUS CIRCUITS WITH APPLICATION TO AN ASYNCHRONOUS MICROPROCESSOR
P I Penzes and A J Martin, California IT, US

1630 POSTERS

6E - 1 BEHAVIOURAL MODELLING OF OPERATIONAL AMPLIFIER FAULTS USING VHDL-AMS
P R Wilson, J N Ross, M Zwolinski and A D Brown, Southampton U, UK
Y Kilic, Philips Semiconductors, UK

6E - 2 A PARALLEL LCC SIMULATION SYSTEM
K Hering, Chemnitz U, DE

6E - 3 ERROR SIMULATION BASED ON THE SystemC DESIGN DESCRIPTION LANGUAGE
F Bruschi, M Chiamenti, F Ferrandi and D Sciuto, Politecnico di Milano, IT

6E - 4 TOWARDS A KERNEL LANGUAGE FOR HETEROGENEOUS COMPUTING
D Björklund and J Lilius, Turku Center for Computer Science (TUCS), FI

1635 BREAK AND POSTER SESSION

6F HOT TOPIC – Deep Submicron Design and Timing Closure

Room F

Moderator/ Organiser: R Otten, TU Eindhoven, NL

Raul Camposano will address an EDA company's view of the DSM problems and how to react to it with tools. From Magma, Patrick Groeneveld will present algorithmic solutions to some of these problems, in particular the nasty ones, such as antenna problems, electromigration, mask enhancement and enabling accurate parasitic prediction and handling. Ralph Otten will give the last part, which picks up the observations and reactions presented by Raul Camposano and the approaches detailed by Patrick Groeneveld, and extrapolate them to derive consequences of these trends in the longer term. These are not mere speculations but really disturbing numbers rigourously derived from laws observed over many years.

1500 R Camposano, Synopsys, US

1530 P Groeneveld, Magma Design Automation, US

1600 R Otten, TU Eindhoven, NL

1630 BREAK AND POSTER SESSION

7A PANEL – Reconfigurable SoC – What Will it Look Like?

Room A

1700-1830
Organiser: D Davis, Actel, US

Moderator: B Lewis, Gartner/Dataquest, US

Panellists: I Bolsens, Xilinx, US
B Gupta, STMicroelectronics, US
R Lauwereins, IMEC, BE
Y Tanurhan, Actel Corporation, US
C Wheddon, Quicksilver Technology, US

The argument against ASIC SoCs is that they have always taken too long and cost too much to design. As new process technologies come on line, the issue of inflexible, unyielding designs fixed in silicon becomes a serious concern. Without the flexibility of reconfigurable logic, will standard cell ASICs disappear and go the way of gate arrays? Will ASIC manufacturers lose their edge in providing intellectual value and become mere purveyors of square die area?

The argument in favour of FPGAs is that they have always provided great design flexibility because they were configurable. The argument against FPGAs is that compared to ASICs they have always been larger, slower and more expensive. Will FPGAs ever become efficient enough to replace ASICs in volume production applications? ASSPs can be designed with partial reconfigurability. Will they become the norm? Or, will new reconfigurable logic cores change the SoC game completely?

1830 CLOSE

7B Layout Aware Logic Synthesis

Room B

Moderators: A Oliveira, INESC, PT
R Murgai, Fujitsu Labs., US

The papers in this session propose innovative algorithms that combine logic synthesis with layout information in order to achieve performance improvements and timing closure in less iterations of the design process. The first two papers are concerned with congestion avoidance during synthesis, the third one addresses synthesis issues under the constant delay model and the last one proposes an algorithm for crosstalk minimisation in dynamic PLAs.

1700 (S) CONGESTION-AWARE LOGIC SYNTHESIS
D Pandini, STMicroelectronics, IT
L Pileggi and A Strojwas, Carnegie Mellon U, US

1715 (S) LAYOUT DRIVEN DECOMPOSITION WITH CONGESTION CONSIDERATION
T Kutschebauch and L Stok, IBM T J Watson Research Center, US

1730 IMPROVING PLACEMENT UNDER THE CONSTANT DELAY MODEL
K Sulimma, W Kunz and I Neumann, Kaiserslautern U, DE
L van Ginneken, Magma Design Automation, US

1800 CROSSTALK ALLEVIATION FOR DYNAMIC PLAs
T-K Tien and T-K Tsai, National Chung Cheng U, ROC
S-C Chang National Tsing Hua U, ROC

1830 CLOSE

7C Buffering and Tapering

Room C

Moderators: J Lienig, Bosch, DE
F Johannes, TU Munich, DE

Getting to the edge of chip performance requires interconnect planning and tapering of transistor networks.

1700 FLIP-FLOP AND REPEATER INSERTION FOR EARLY INTERCONNECT PLANNING
R Lu, G Zhong and C-K Koh, Purdue U, US
K-Y Chao, Intel Corporation, US

1730 (S) CONGESTION ESTIMATION WITH BUFFER PLANNING IN FLOORPLAN DESIGN
W C Wong, C W Sham and F Y Young, The Chinese U, HK

1745 (S) MAZE ROUTING WITH BUFFER INSERTION UNDER TRANSITION TIME CONSTRAINTS
L-D Huang, M L Lai and D F Wong, Texas U at Austin, US
Y X Gao, Avanti Corporation, US

1800 OPTIMAL TRANSISTOR TAPERING FOR HIGH-SPEED CMOS CIRCUITS
L Ding and P Mazumder, Michigan U, Ann Arbor, US

1830 CLOSE

7D Automatic Design Debug and TPG

Room D

Moderators: P Teixeira, INESC-IST, PT
B Straube, FhG IIS/EAS Dresden, DE

Papers deal with automatic diagnosis for design debug, test pattern generation for delay faults and a novel methodology for hierarchical and functional test generation.

1700 INCREMENTAL DIAGNOSIS AND DEBUGGING OF MULTIPLE FAULTS AND ERRORS
A Veneris, B Liu and M Amiri, Toronto U, CA
M Abadir, Motorola, UA

1730 TEST ENRICHMENT FOR PATH DELAY FAULTS USING MULTIPLE SETS OF TARGET FAULTS
I Pomeranz, Purdue U, US
S M Reddy, Iowa U, US

1800 FACTOR: A HIERARCHICAL METHODOLOGY FOR FUNCTIONAL TEST GENERATION AND TESTABILITY ANALYSIS
V M Vedula and J A Abraham, Texas U, Austin, US

1830 CLOSE

7E Object Oriented System Specification and Design

Room E

Moderators: W Grass, Passau U, DE
E Villar, Cantabria U, ES

This session presents several aspects of object oriented techniques for system specification and design. The first paper addresses the problem of composing compiled C++ objects to construct an executable system model. The second paper proposes constraint solving for functional verification. The last two papers address full system level specification and design including hardware-software, analogue and digital functions.

1700 AN ENVIRONMENT FOR DYNAMIC COMPONENT COMPOSITION FOR EFFICIENT CO-DESIGN
F Doucet, S Shukla and R Gupta, UC Irvine, US
M Otsuka, Fujitsu, JP

1730 FUNCTIONAL VERIFICATION FOR SystemC DESCRIPTIONS USING CONSTRAINT SOLVING
F Ferrandi, M Rendine and D Sciuto, Politecnico di Milano, IT

1800 (S) THE CO-DESIGN OF SoC-BASED EMBEDDED SYSTEMS USING HASoC
M D Edwards and P N Green, UMIST, UK

1815 (S) A FUNCTIONAL SPECIFICATION NOTATION FOR CO-DESIGN OF MIXED ANALOG – DIGITAL SYSTEMS
A Doboli, New York State U, US
R Vemuri, Cincinnati U, US

1830 CLOSE

7F Design Case Studies (Designers' Forum)

Room F

Moderator: K Dioury, Avertec, FR
This session presents different design studies, considering the issues of verification, fast prototyping, simulation and reconfiguration.

1700 (S) A LOW-POWER LINE DRIVER USING RESONANT CHARGING
C Schlachta, B Voss and M Glesner, TU Darmstadt, DE

1715 (S) MIXED-SIGNAL SIMULATION AT DIFFERENT LEVELS OF ABSTRACTION OF AN EMBEDDED FLASH MACROCELL BASED DESIGN IN 0.18um NON VOLATILE MEMORIES TECHNOLOGY
P Daglio, G Guatini and C Roma, STMicroelectronics, IT

1730 (S) THE USE OF DYNAMICALLY RECONFIGURABLE FPGAs TO ACHIEVE REAL TIME IMAGE ROTATION
E-B Bourennane, S Bouchoux, C Milan and M Paindavoine, Burgundy U, FR

1745 (S) ELECTRICAL CHARACTERIZATION AND RELATED PERFORMANCES
F De Pieri, M Ferloni, R Gaio, M Grassi, C Meani and M Pavesi, Italtel, IT
B Bazille and P Deroux-Dauphin, Temento Systems, FR

1800 (S) DESIGN OF A REED SOLOMON DECODER USING PARTIAL DYNAMIC RECONFIGURATION OF XILINX VIRTEX FPGAs – A CASE STUDY
A Haase, R Siegmund, C Kretzschmar, D Mueller, J Schneider, M Boden and M Langer, Fh G IIS/EAS Dresden, DE

1815 (S) USING MODEL CHECKING TECHNIQUES FOR DEBUGGING A DATA CACHE MANAGEMENT BLOCK
J Blasquez and S Lassere, Texas Instruments, FR
C Chapuy, S Delacherie, G Nguyen and I Moussa, TNI-Valiosys, FR

1830 CLOSE

THURSDAY 7 MARCH, 2002

8A HOT TOPIC - UML: Using the Unified Modeling Language for Embedded System Specification

Room A

Moderator/ Organiser: L Lavagno, Politecnico di Torino, IT

The UML is emerging as a promising standard to flexibly capture a broad range of requirements for electronic systems. Its graphical notations allow one to describe semi-formally the intended behaviour of a system and constraints on its implementation. Although tool support to computer-aided refinement of such specifications is still lagging, there are promising proposals to make it a viable option also for hardware and software implementations. This tutorial will cover various aspects of how the UML can be used for both specification and implementation of embedded electronic systems.

0900 THE REAL-TIME UML STANDARD: DEFINITION AND APPLICATION
B Selic, Rational Inc, US

0930 UML FOR EMBEDDED SYSTEMS SPECIFICATION AND DESIGN: MOTIVATION AND OVERVIEW
G Martin, Cadence Design Systems, US

1000 A UML-BASED DESIGN METHODOLOGY FOR REAL-TIME AND EMBEDDED SYTEMS
G de Jong, Telelogic Inc, BE

1030 BREAK

8B Real-Time Embedded Systems

Room B

Moderators: Z Peng, Linkoping U, SE
J Sifakis, VERIMAG, FR

The session deals with modelling and analysis of embedded real-time systems. The first two papers address the issue of voltage scheduling. The third paper deals with generating property preserving abstractions of synchronous real-time programs.

0900 AN OPTIMAL VOLTAGE SCHEDULE FOR REAL-TIME SYSTEMS ON A VARIABLE VOLTAGE PROCESSOR
G Quan and X Hu, Notre Dame U, US

0930 A DYNAMIC VOLTAGE SCALING ALGORITHM FOR DYNAMIC-PRIORITY HARD REAL-TIME SYSTEMS USING SLACK TIME ANALYSIS
W Kim, J Kim and S L Min, Seoul National U, KR

1000 EXTENDING SYNCHRONOUS LANGUAGES FOR GENERATING ABSTRACT REAL-TIME MODELS
G Logothetis and K Schneider, Karlsruhe U, DE

1030 POSTERS

8B - 1 A NEW TIME MODEL FOR THE SPECIFICATION, DESIGN, VALIDATION AND SYNTHESIS OF EMBEDDED REAL-TIME SYSTEMS
R Muenzenberger, M Doerfel, F Slomka and R Hofmann, Erlangen U, DE

8B - 2 IMPROVED CONSTRAINTS FOR MULTIPROCESSOR SYSTEM SCHEDULING
M Grajcar and W Grass, Passau U, DE

1035 BREAK

8C Interconnect Modelling

Room C

Moderators: J Phillips, Cadence Berkeley Labs, US
L M Silveira, IST/INESC, PT

This session presents recent work in the modelling of interconnect and crosstalk. The first paper presents a methodology for introducing transmission lines into an analogue mixed-signal flow. The second paper introduces metrics for capacitive coupling crosstalk noise. The third and fourth papers discuss computing dominant poles for reduced order admittance matrices and library compatible capacitance models for gate-level timing verification.

0900 AN INTERCONNECT-AWARE METHODOLOGY FOR ANALOG AND MIXED SIGNAL DESIGN, BASED ON HIGH BANDWIDTH (OVER 40 GHz) ON-CHIP TRANSMISSION LINE APPROACH
D Goren, M Zelikson, T C Galambos, R Gordin, B Livshitz, A Amir, A Sherman and I A Wagner, IBM, ISR

0930 CLOSED-FORM CROSSTALK NOISE METRICS FOR PHYSICAL DESIGN APPLICATIONS
L H Chen, Avant! Corp, US
M Marek-Sadowska, UC Santa Barbara, US

1000 (S) FORMULATION OF LOW-ORDER DOMINANT POLES FOR Y-MATRIX OF INTERCONNECTS
Q Xu and P Mazumder, Michigan U, US

1015 (S) LIBRARY COMPATIBLE Ceff FOR GATE-LEVEL TIMING
B Sheehan, Mentor Graphics, US

1030 POSTERS

8C - 1 ON-CHIP INDUCTANCE MODELS: 3D OR NOT 3D?
T Lin, M W Beattie and L T Pileggi, Carnegie Mellon U, US

8C - 2 IMPROVING THE ACCURACY OF POWER GRID SIMULATION
S R Nassif, IBM, US

1035 BREAK

8D On-Line Testing and Fault Tolerance

Room D

Moderators: L Bouzaida, STMicroelectronics, FR
A D Singh. Auburn U, US

On-line detection of power supply noise, dependability improvement insertion at RT level, concurrent error detection exploiting idle cycles, and fault injection approaches are covered in this session.

0900 SELF-CHECKING SCHEME FOR THE ON-LINE TESTING OF POWER SUPPLY NOISE
C Metra L Schiano and B Ricco, DEIS – Bologna U, IT
M Favalli, DI – Ferrara U, IT

0930 AUTOMATIC MODIFICATIONS OF HIGH LEVEL VHDL DESCRIPTIONS FOR FAULT DETECTION OR TOLERANCE
R Leveugle, TIMA, Grenoble, FR

1000 (S) EXPLOITING IDLE CYCLES FOR ALGORITHM LEVEL RE-COMPUTING
K Wu and R Karri, Brooklyn Polytechnic U, US

1015 (S) NEW TECHNIQUES FOR SPEEDING-UP FAULT-INJECTION CAMPAIGNS
L Berrojo and I Gónzalez, Alcatel Espacio, ES
F Corno, M Sonza Reorda and G Squillero, Politecnico di Torino, IT
L Entrena and C López, Carlos III de Madrid U, ES

1030 POSTERS
8D - 1 A FAST JOHNSON-MOBIUS ENCODING SCHEME FOR FAULT SECURE BINARY COUNTERS
K S Papadomanolakis, A P Kakarountas, N Sklavos and C E Goutis, Patras U, GR

8D - 2 A NOVEL METHODOLOGY FOR THE CONCURRENT TEST OF PARTIAL AND DYNAMICALLY RECONFIGURABLE SRAM-BASED FPGAs
M G Gericota and G R Alves, ISEP, PT
M L Silva and J M Ferreira, FEUP/INESC, PT

8D - 3 EFFICIENT ON-LINE TESTING METHOD FOR A FLOATING-POINT ITERATIVE ARRAY DIVIDER
A Drozd, M Lobachev and J Drozd, Odessa State Polytechnic U, UKR

1035 BREAK

8E Design Space Evaluation

Room E

Moderators: J Teich, Paderborn U, DE
W Kruijtzer, Philips Research, NL

This session is devoted to the analysis of high-level trade-offs in system level design. The first paper discusses an abstract model for exploring different mappings from function to architecture. The second paper describes techniques for high-level area and delay estimation for FPGA implementations from matlab sources. The last two papers examine issues in design space exploration and simulation performance optimisation in C/C++ -based design environments.

0900 SYSTEM DESIGN FOR FLEXIBILITY
C Haubelt and J Teich, Paderborn U, DE
K Richter, TU Braunschweig, DE

0930 ACCURATE AREA AND DELAY ESTIMATORS FOR FPGAs
A Nayak, M Haldar, A Choudhary and P Banerjee, Northwestern U, US

1000 (S) A POWERFUL SYSTEM DESIGN METHODOLOGY COMBINING OCAPI AND HANDEL-C FOR CONCEPT ENGINEERING
K Buchenrieder, A Pyttel and A Sedlmeier, Infineon Technologies, DE

1015 (S) AUTOMATED CONCURRENCY RE-ASSIGNMENT IN HIGH LEVEL SYSTEM MODELS FOR EFFICIENT SYSTEM-LEVEL SIMULATION
N Savoiu, S Shukla and R Gupta, UC Irvine, US

1030 POSTER
8E - 1 TOP-DOWN SYSTEM LEVEL DESIGN METHODOLOGY USING SpecC, VCC AND SystemC
L Cai and D Gajski, UC Irvine, US
P Kritzinger and M Olivarez, Motorola, US

1035 BREAK

8F System Design Case Studies (Designers' Forum)

Room F

Moderator: M Engels, IMEC, BE

This session presents different real case system design implementations.

0900 (S) HW/SW INTERFACES DESIGN OF A VDSL MODEM USING AUTOMATIC REFINEMENT OF A VIRTUAL ARCHITECTURE SPECIFICATION INTO A MULTIPROCESSOR SoC: A CASE STUDY
W Cesario, Y Paviot, A Baghdadi, L Gauthier, D Lyonnard, G Nicolescu, S Yoo and A A Jerraya, TIMA, Grenoble, FR
M Diaz Nava, STMicroelectronics, FR

0915 (S) DEVELOPMENT OF A SINGLE CHIP SPEECH RECOGNITION SYSTEM USING A HW/SW CODESIGN METHODOLOGY
S Bocchio, A Rosti, M Borgatti, L Cali', M Besana and F Lertora, STMicroelectronics, IT

0930 (S) A DUAL-PROCESSOR SYSTEM-ON-CHIP FOR ELECTRONICS CARTHOGRAPHIC APPLICATIONS: A DESIGN CASE STUDY
L Fanucci, CSMDR, IT
L Bertini, Pisa U, IT
M De Marinis, Pisa Research Consortium, IT

0945 (S) SATELLITE TUNER SINGLE CHIP SIMULATION WITH ADVANCED DESIGN SYSTEM
P Busson, A Moutard, B Louis-Gavet, P Dautriche, F Lemery, C Pujol and J-P Morin, STMicroelectronics, FR

1000 (S) FAST ETHERNET MEDIA ACCESS CONTROLLER CORE
G Paya, M Martinez-Peiro, F J Ballester, R Gadea and V Herrero, UP Valencia, ES

1015 (S) VIRTUAL SoC PROTOTYPING: CASE STUDY FOR A TRANSACTIONAL MODEL OF AN USB DRIVER
V Amadio, M Caldari, M Conti, E Corinti, P Crippa, S Orcioni and C Turchetti, Ancona U, IT
M Coppola, STMicroelectronics, FR

1030 BREAK

9A HOT TOPIC – From System Specification to Layout: Seamless Top-Down Design Methods for Analogue and Mixed Signal Applications

Room A

Moderators/ Organisers: I Rugen-Herzig, Infineon Technolgies, DE
R Sommer, Infineon Technologies, DE

The session is dedicated to latest R&D activities within the MEDEA+ project ANASTASIA+. Main focus will be the development of seamless top-down design methods for integrated analogue and mixed-signal systems and to achieve a high level of automation and reuse in the A/MS design process. These efforts are motivated by the urgent need to close the current gap in the industrial design flow between system specification and design on the one hand and block-level circuit design on the other hand.

1100 TOP-DOWN DESIGN FLOW – APPLICATIONS FROM CIRCUIT SIZING, DESIGN CENTERING, AND AUTOMATED BEHAVIORAL MODELING
R Sommer, M Thole and E Hennig, Infineon Technologies, DE

1130 MODELING AND SIMULATION OF SPECIFIC FUNCTIONALITIES – SIGMA-DELTA
U Gatti, Siemens ICN, IT
P Malcovati, Pavia U, IT
F Maloberti, Texas A&M U, US

1200 MIXED-SIGNAL SYSTEM ON CHIP DESIGN ENVIRONMENT
C Einwich, C Clauss and P Schwarz, FhG IIS/EAS Dresden, DE
G Noessing, Infineon Technologies, AT

1230 LUNCH

9B Architectural Level Synthesis

Room B

Moderators: P Eles, Linkoping U, SE
B Mesman, Philips/TU Eindhoven, NL

This session presents new research on design exploration, at the architectural level, oriented to the synthesis of application specific memory systems and datapaths.

1100 MEMORY SYSTEM CONNECTIVITY EXPLORATION
P Grun, N Dutt and A Nicolau, UC Irvine, US

1130 PERFORMANCE-AREA TRADE-OFF ADDRESS GENERATORS FOR ADDRESS DECODER-DECOUPLED MEMORY
S Hettiaratchi, P Y K Cheung and T J W Clarke, Imperial College, UK

1200 MULTIPLE-PRECISION CIRCUITS ALLOCATION INDEPENDENT OF DATA-OBJECTS LENGTH
M C Molina, J M Mendias and R Hermida, Madrid Complutense U, ES

1230 POSTERS

9B - 1 COMPILE-TIME AREA ESTIMATION FOR FPGA-BASED RECONFIGURABLE SYSTEMS
D Kulkarni and W A Najjar, UC Riverside, US
R Rinker, Idaho U, US
F J Kurdahi, UC Irvine, US

9B - 2 MAXIMIZING CONDITONAL REUSE BY PRE-SYNTHESIS TRANSFORMATIONS
O Penalba, J M Mendias and R Hermida, Madrid Complutense U, ES

9B - 3 CONTROL CIRCUIT TEMPLATES FOR ASYNCHRONOUS BUNDLED-DATA PIPELINES
S Tugsinavisut and P A Beerel, Southern California U, US

1235 LUNCH

9C Advanced Linear Modelling Techniques

Room C

Moderators: P Feldmann, Celight Inc, US
G Vandersteen, IMEC, BE

This session brings together a number of papers on system modelling. The first paper addresses the problem of time-varying linear system modelling. It introduces an efficient Krylov subspace based reduction which uses time-domain integration for linear operator evaluation. The second paper presents a technique to generate passive rational models for systems characterised in the frequency domain. The last paper describes a model reduction technique which approximates the time domain response using Laguerre polynomials.

1100 EFFICIENT MODEL REDUCTION OF LINEAR TIME-VARYING SYSTEMS VIA COMPRESSED TRANSIENT SYSTEM FUNCTION
E Gad and M Nakhla, Carleton U, CA

1130 PASSIVE CONSTRAINED RATIONAL APPROXIMATION ALGORITHM USING NEVANLINNA-PICK INTERPOLATION
C P Coelho and L M Silveira, IST/INESC/Cadence European Laboratories, PT
J R Phillips, IST/TU Lisbon, PT

1200 MODEL REDUCTION IN THE TIME-DOMAIN USING LAGUERRE POLYNOMIALS AND KRYLOV METHODS
Y Chen, V Balakrishnan, C-K Koh and K Roy, Purdue U, US

1230 POSTERS

9C - 1 SIMPLE AND EFFICIENT APPROACH FOR SHUNT ADMITTANCE PARAMETERS CALCULATIONS OF VLSI ON-CHIP INTERCONNECTS ON SEMICONDUCTING SUBSTRATE
H Ymeri, B Nauwelaers and S Vandenberghe, KU Leuven, BE
K Maex, D De Roest and M Stucchi, IMEC, BE

9C - 2 COMPACT MACROMODEL FOR LOSSY COUPLED TRANSMISSION LINES
R Khazaka and M Nakhla, Carleton U, CA

9C - 3 A STANDARD MODEL FOR PREDICTING THE PARASITIC
S Baffreau and E Sicard, INSA, FR
S Calvet, Motorola, FR
C Huet, Airbus, FR
C Marot, Siemens, FR

9C - 4 EMC DESIGN METHOD OF HIGH-DENSITY INTEGRATED CIRCUITS
J-L Levant, Atmel, FR
M Ramdani, ESEO, FR

1235 LUNCH

9D Memory Testing and ATPG Issues

Room D

Moderators: H Obermeir, Infineon Technologies, DE
M Sonza Reorda, Politecnico di Torino, IT

The first two papers introduce new test techniques for memories; the following two address the issues of untestable fault identification and test oriented modelling.

1100 AN OPTIMAL ALGORITHM FOR THE AUTOMATIC GENERATION OF MARCH TESTS
A Benso, S Di Carlo, G Di Natale and P Prinetto, Politecnico di Torino, IT

1130 (S) MINIMAL TEST FOR DETECTING STATE COUPLING FAULTS IN MEMORIES
A J van de Goor, TU Delft, NL
M S Abadir and A Carlin, Motorola, US

1145 (S) MAXIMIZING IMPOSSIBILITIES FOR UNTESTABLE FAULT IDENTIFICATION
M S Hsiao, Virginia Tech, US

1200 AUTOMATED MODELING OF CUSTOM DIGITAL CIRCUITS FOR TEST
S Bose, Intel Corporation, US

1230 LUNCH

9E Embedded Software Performance Analysis and Optimisation

Room E

Moderators: H Hsieh, UC Riverside, US
R Lauwereins, IMEC, BE

This session deals with the important issue of software development for embedded systems. The session will start with a discussion of scheduling, and identifying false path in scheduling analysis. Next, the related issue of performance estimation is presented. Lastly, the session closes with two short papers on cache optimisation.

1100 FALSE PATH ELIMINATION IN QUASI-STATIC SCHEDULING
G Arrigoni, L Duchini and C Passerone, Politecnico di Torino, IT
L Lavagno, Politecnico di Torino, IT
Y Watanabe, Cadence Design Systems, US

1130 A DATA ANALYSIS METHOD FOR SOFTWARE PERFORMANCE PREDICTION
G Bontempi, IMEC, BE
W Kruijtzer, Philips Research, NL

1200 (S) A CODE TRANSFORMATION-BASED METHODOLOGY FOR IMPROVING I-CACHE PERFORMANCE OF MULTIMEDIA APPLICATIONS
N Liveris, Northwestern U, US
N D Zervas, ALMA Technologies, GR
D Soudris , Thrace Democritus U, GR
C E Goutis, Patras U, GR

1215 (S) A COMPILER-BASED APPROACH FOR IMPROVING INTRA-ITERATION DATA REUSE
M T Kandemir, Pennsylvania State U, US

1230 POSTERS

9E - 1 AUTOMATIC TOPOLOGY-BASED IDENTIFICATION OF INSTRUCTION-SET EXTENSIONS FOR EMBEDDED PROCESSORS
L Pozzi, M Vuletic and P Ienne, EPFL, CH

9E - 2 TUNING PLATFORMS WITH CONFIGURABLE VOLTAGE AND CACHE
T Givargis, UC Irvine, US
F Vahid and J Villarreal, UC Riverside, US

1235 LUNCH

9F Testing and Design for Testability Methodologies (Designers' Forum)

Room F

Moderator: F Fummi, Verona U, IT

This session highlights the application of design for testability techniques to real designs and problems related to designing testable and fault tolerant actual systems.

1100 (S) CONSTRAINED LOGIC BIST FOR MICROPROCESSORS
S Kundu, S Sengupta, D Goswami and R Galivanche, Intel Corporation, US

1115 (S) A BIST: TESTING EXTERNAL MEMORIES AND THEIR INTERCONNECTS
H Kim, X Gu and S Chung, Cisco Systems, US

1130 (S) A LOW-OVERHEAD SCAN-BASED BIST TECHNIQUE BASED ON DATA REINSTATE METHOD TO TEST EMBEDDED SRAMs IN MAJC MICROPROCESSOR
R Pendurkar, Sun Microsystems, US

1145 (S) MULTI-PORT G.shdsl DFT FEATURES
C M Bui, Centillium Communications, US

1200 (S) DESIGNING A LOW POWER FAULT-TOLERANT MICROCONTROLLER FOR MEDICINE INFUSION DEVICES
A P Kakarountas, K S Papadomanolakis, V Spiliotopoulos and C E Goutis, Patras U, GR
S Nikolaidis, Thesalloniki U, GR

1215 (S) HIGH-RESOLUTION TIMING MEASUREMENT SYSTEM
B M Rogina, Rudjer Boskovic Institute, CR

1230 LUNCH

9G TECHNICAL PLENARY – 40 Years of EDA

Room G

1345 – 1430

Moderator: A Jerraya, TIMA, Grenoble, FR

EUROPEAN CAD FROM THE 60'S TO THE NEW MILLENIUM
Joseph Borel, J.B.-R&D Consulting, FR

CAD has always been hardly understood by the CEO's of companies because it obeys rules (if any) very different from the process. A rich variety of CAD and TCAD solutions have been developed in Europe in the early days of the CAD industry. These solutions have come to introduce real innovations in the field, but because they were mostly internal to the companies they have never reached the proper engineering level that would have enabled their introduction in the market. A review of the CAD history activity in Europe will be presented in this Plenary Session, together with some prospects on how it could evolve in the coming years and change from its lackluster industrial visibility

10A HOT TOPIC – Design Technology for Networked Reconfigurable FPGA Platforms

Room A

Organiser/ Moderator: I Bolsens, Xilinx, US

Speakers: D Verkest, IMEC, BE
S Guccione, Xilinx, US
S Singh, Xilinx, US

1430-1600

Internet has become a driving force for the deployment of embedded systems. Software embedded systems often do not offer the best solution in terms of cost, speed and power. It will be demonstrated in this session that FPGA platforms create a good compromise between high performance and maintaining the capability of networked reconfiguration. During the first part of the presentation we will discuss a user scenario of networked reconfigurable hardware. An appliance equipped with a reconfigurable FPGA platform localises a reconfiguration server.

This session will explain the future capabilities of the above methodology and the requirements wrt future design technology. We will highlight the need of higher level design methods and tools in order to make the transparent mapping of an application onto a mixed hardware/software platform possible as well as the need for high speed dynamic reconfiguration on multiple FPGA platforms.

1600 CLOSE

10B High-Level Synthesis and Asynchronous Pipelines

Room B

Moderators: N Dutt, UC Irvine, US
M Renaudin, TIMA, Grenoble, FR

The first two papers present new templates to build fine-grain high-speed asynchronous pipelines using different approaches for completion detection. The next two papers address low-power and instruction set synthesis.

1430 HIGH-SPEED NON-LINEAR ASYNCHRONOUS PIPELINES
R O Ozdag and P A Beerel, Southern California U, US
M Singh, UNC, US
S M Nowick, Columbia U, US

1500 (S) SINGLE-TRACK ASYNCHRONOUS PIPELINE TEMPLATES USING 1-OF-N ENCODING
M Ferretti and P A Beerel, Southern California U, US

1515 (S) POWER-MANAGEABLE SCHEDULING TECHNIQUE FOR CONTROL DOMINATED HIGH-LEVEL SYNTHESIS
C Chen, Windsor U, CA
M Sarrafzadeh, UC Los Angeles, US

1530 (S) PRACTICAL INSTRUCTION SET AND COMPILER DESIGN USING STATIC RESOURCE MODEL
Q Zhao, TU Eindhoven, NL

1545 CLOSE

10C Coupling and Switching Noise Modelling within Integrated Circuits

Room C

Moderators: E Sicard, INSA, FR
G Vandenbosch, KU Leuven, BE

This session deals with parasitic coupling effect and switching noise analysis within integrated circuits. Concerning coupling analysis, a hierarchical substrate coupling tool is proposed for interference reduction, and a fast method for coupling simulation within microwave circuits is presented. Secondly, an accurate estimation technique is proposed for switching noise analysis, and a macro modelling approach for i/o switching is presented, for signal integrity simulation.

1430 HIERARCHICAL SIMULATION OF SUBSTRATE COUPLING IN MIXED-SIGNAL ICs CONSIDERING THE POWER SUPPLY NETWORK
T Brandtner, Infineon Technologies, AT
R Weigel, Linz U, AT

1500 FAST METHOD TO INCLUDE PARASITIC COUPLING IN CIRCUIT SIMULATIONS
B L A Van Thielen and G A E Vandenbosch, KU Leuven, BE

1530 (S) ACCURATE ESTIMATING SIMULTANEOUS SWITCHING NOISES BY USING APPLICATION SPECIFIC DEVICE MODELING
L Ding and P Mazumder, Michigan U, US

1545 (S) MACROMODELING OF DIGITAL I/O PORTS FOR SYSTEM EMC ASSESSMENT
I S Stievano, F G Canavero and I A Maio, Politecnico di Torino, IT
Z Chen, B Becker and G Katopis, IBM, US

1600 CLOSE

10D PANEL – Formal Verification Techniques: Industrial Status and Perspectives

Room D

1430-1600
Organiser: I Moussa, TNI-Valiosys, FR

Moderator: R Pacalet, ENST Paris, FR

Panellists: J Blasquez, Texas Instruments, Villeneuve-Loubet, FR
M van Hulst, Philips, Eindhoven, NL
A Fedeli, STMicroelectronics, Agrate, IT
J-L Lambert, TNI-Valiosys, FR
D Borrione, TIMA-UJF, FR
C Hanuch, Verisity, FR
P Bricaud, Mentor Graphics, FR
S Meier, Synopsys, US

Design verification presents the biggest bottleneck in digital hardware design. Major hardware bugs found in ASIC design may cause expensive project delays when they are discovered during system test on the real silicon chip. The consequences are severe, from cost over-runs to lost market opportunity. Simulation and emulation tools, which are traditionally used to find bugs in a design, often cannot find the corner cases or hard-to-find bugs that may occur only after hundreds of thousands of cycles, and are well beyond the reach of conventional simulation and emulation technologies. Formal methods have emerged as an alternative approach to ensure the quality and correctness of hardware designs, overcoming some of the limitations of traditional validation techniques such as simulation and testing.

1630 CLOSE

10E Power Optimisation for Embedded Processors

Room E

Moderators: W Fornaciari, Politecnico di Milano, IT
L Lavagno, Politecnico di Torino, IT

The focus of this session is on the most important aspects impacting the power budget of embedded processors. The session will address the analysis of operation complexity, procedure inlining, bus and cache encoding/timing.

1430 LOW POWER EMBEDDED SOFTWARE OPTIMIZATION USING SYMBOLIC ALGEBRA
A Peymandoust, T Simunic and G De Micheli, Stanford U, US

1500 AN ADAPTIVE DICTIONARY ENCODING SCHEME FOR SoC DATA BUSES
T Lv and W Wolf, Princeton U, US
J Henkel and H Lekatsas, NEC, US

1530 (S) POWER EFFICIENT EMBEDDED PROCESSOR IP's THROUGH APPLICATION-SPECIFIC TAG COMPRESSION IN DATA CACHES
P Petrov and A Orailoglu, UC San Diego, US

1545 (S) SYSTEMATIC POWER-PERFORMANCE TRADE-OFF IN MPEG-4 BY MEANS OF SELECTIVE FUNCTION INLINING STEERED BY ADDRESS OPTIMISATION OPPORTUNITIES
M Palkovic, M Miranda and F Catthoor, IMEC, BE

1600 CLOSE

10F Analogue and Mixed-Signal Design (Designers' Forum)

Room F

Moderatos: C Dufaza, LIRMM, FR

This session will present some design experiences for analogue circuits sizing and two design methodologies for the analysis of analogue and mixed-signal circuits.

1430 (S) DESIGN OF A BROADBAND SD MODULATOR IN 2.5-V CMOS
R del Rio, F Medeiro, J M de la Rosa, B Perez-Verdu and A Rodriguez-Vazquez, IMSE-CNM, ES

1445 (S) TECHNOLOGY MIGRATION OF A HIGH-PERFORMANCE CMOS AMPLIFIER USING AN AUTOMATED FRONT-TO-BACK ANALOG DESIGN FLOW
S Dugalleix and F Lemery, STMicroelectronics, FR
A Shah, Neolinear Inc, US

1500 (S) AN AUTOMATED APPROACH FOR SIZING COMPLEX ANALOG CIRCUITS IN A SIMULATION-BASED FLOW
E Hennig and R Sommer, Infineon Technologies, DE
L Charlack, Neolinear Inc, US

1515 (S) A FRAMEWORK FOR ANALYSIS OF SUBSTRATE COUPLING METHODS FOR MIXED-SIGNAL CIRCUITS
J P Amaro, INESC, PT
J R Phillips, Cadence Berkeley Labs, US
L M Silveira, INESC/Cadence European Labs, PT

1530 (S) SYMBOLIC ANALYSIS IN ANALOG IC DESIGN: A VIEW FROM THE INDUSTRIAL CAD PERSPECTIVE
E Hennig and R Sommer, Infineon Technologies, DE

1545 (S) STASTICAL CORNER MODELS FOR ROBUST DESIGN
M Kocher and G Rappitsch, Autriamicrosystems, AT

1600 CLOSE

POSTER SESSIONS

LEVEL 2 – CONFERENCE ROOM FOYER

Please see below the complete list of Posters which will be presented during the Conference. All posters will be shown during the 3 days of the Conference. Authors will be standing by their posters during the two breaks on Wednesday and at the break immediately after the session in which the Poster is presented. Authors will also be able to introduce their Poster during their sessions, using one summary slide. The posters will be conveniently located just outside the lecture theatre in which they are presented. The boards are numbered with the relevant session number first, i.e. 1B, 5B, 7C and followed by the Poster's individual number within that session, i.e. – 1, - 2, - 3.

1B – 1 AN APPROACH TO MODEL CHECKING FOR NONLINEAR ANALOG SYSTEMS
W Hartong, L Hedrich and E Barke, Hannover U, DE

2B – 1 SPEEDING UP SAT FOR EDA
S Pilarski and G Hu, Synopsys, US

2B – 2 SEARCH-BASED SAT USING ZERO-SUPPRESSED BDDS
F A Aloul, M N Mneimneh and K A Sakallah, Michigan U, US

3B – 1 AN ENCODING TECHNIQUE FOR LOW POWER CMOS IMPLEMENTATIONS OF CONTROLLERS
M Martinez, M J Avedillo, J M Quintana, M Koegst, S T Ruelke and H Susse, CNM-IMSE, ES

3B – 2 COMPOSITION TREES IN FINDING BEST VARIABLE ORDERINGS FOR ROBDDS
E Dubrova, Royal IT, SE

1C – 2 A NEW FORMULATION FOR SOC FLOORPLAN AREA MINIMIZATION PROBLEM
C-H Lee, Y-C Lin, W-Y Fu, C-C Chang and T-M Hsieh, Chung-Yuan Christian U, ROC

1C - 3 NON-RECTANGULAR SHAPING AND SIZING OF SOFT MODULES FOR FLOORPLAN DESIGN IMPROVEMENT
C C N Chu, F Y Young and W S Luk, The Chinese U, HK

2C – 1 EZ ENCODING: A CLASS OF IRREDUNDANT LOW POWER CODES FOR DATA ADDRESS AND MULTIPLEXED ADDRESS BUSES
Y Aghaghiri and M Pedram, Southern California U, US
F Fallah, Fujitsu Labs of America, US

2C – 2 ESTIMATION OF POWER CONSUMPTION IN ENCODED DATA BUSSES
A Garcia, L D Kabulepa and M Glesner, TU Darmstadt, DE

3C – 1 OPTIMIZATION TECHNIQUES FOR DESIGN OF GENERAL AND FEEDBACK LINEAR ANALOG AMPLIFIER WITH SYMBOLIC ANALYSIS
T C Hieu and E-H Horneber, TU Braunschweig, DE

3C – 2 CRITICAL COMPARISON AMONG SOME ANALOG FAULT DIAGNOSIS PROCEDURES BASED ON SYMBOLIC TECHNIQUES
A Luchetta, Basilicata C. da Macchia U, IT
S Manetti and M C Piccirilli, Florence U, IT

4C – 1 THE SELECTIVE PULL-UP (SP) NOISE IMMUNITY SCHEME FOR DYNAMIC CIRCUITS
M R Stan and A Panigrahi, Virginia U, US

4C – 2 DESIGN AND VALIDATION FLOW INCLUDING SUBSTRATE PARASITIC EXTRACTION FOR RF CIRCUITS
A Cathelin, D Saias and D Belot, STMicroelectronics, FR
Y Leclercq and F Clement, Simplex Solutions, FR

4C – 3 A COMPLETE PHASE-LOCKED LOOP POWER CONSUMPTION MODEL
D Duarte, V Narayanan and M J Irwin, The Pennsylvania State U, US

5C – 1 STATISTICAL TIMING DRIVEN PARTITIONING FOR VLSI CIRCUITS
C Ababei and K Bazargan, Minnesota U, US

6C – 1 DAISY-CT: A HIGH-LEVEL SIMULATION TOOL FOR CONTINUOUS-TIME DS MODULATORS
K Francken, M Vogels, E Martens and G Gielen, KU Leuven, BE

6C - 2 AUTOMATED OPTIMAL DESIGN OF SWITCHED-CAPACITOR CIRCUITS
A Hassibi and M Hershenson, Barcelona Design, ES

8C – 1 ON-CHIP INDUCTANCE MODELS: 3D OR NOT 3D?
T Lin, M W Beattie and L T Pileggi, Carnegie Mellon U, US

8C – 2 IMPROVING THE ACCURACY OF POWER GRID SIMULATION
S R Nassif, IBM, US

9C – 1 SIMPLE AND EFFICIENT APPROACH FOR SHUNT ADMITTANCE PARAMETERS CALCULATIONS OF VLSI ON-CHIP INTERCONNECTS ON SEMICONDUCTING SUBSTRATE
H Ymeri and S Vandenberghe, KU Leuven, BE
K Maex, D De Roest and M Stucchi, IMEC, BE

9C – 2 COMPACT MACROMODEL FOR LOSSY COUPLED TRANSMISSION LINES
R Khazaka and M Nakhla, Carleton U, CA

9C – 3 A STANDARD MODEL FOR PREDICTING THE PARASITIC
S Baffreau and E Sicard, INSA, FR
S Calvet, Motorola, FR
C Huet, Airbus, FR
C Marot, Siemens, FR

9C – 4 EMC DESIGN METHOD OF HIGH-DENSITY INTEGRATED CIRCUITS
J-L Levant, Atmel, FR
M Ramdani, ESEO, FR

1D – 1 FINDING A COMMON FAULT RESPONSE FOR DIAGNOSIS DURING SILICON DEBUG
I Pomeranz, Purdue U, US
J Rajski, Mentor Graphics, US
S M Reddy, Iowa U, US

1D –2 IDDT TESTING OF EMBEDDED CMOS SRAMs
S A Kumar, R Z Makki and D Binkley, North Carolina U, Charlotte, US

1D – 3 FAULT DETECTION AND DIAGNOSIS USING WAVELET BASED TRANSIENT CURRENT ANALYSIS
S Bhunia and K Roy, Purdue U, US

2D – 1 AN EFFICIENT TEST AND DIAGNOSIS SCHEME FOR THE FEEDBACK TYPE OF ANALOG CIRCUITS WITH MINIMAL ADDED CIRCUITS
J W Lin and C L Lee, National Chiao Tung U, ROC
J-E Chen, Chung Hwa U, ROC

2D – 2 ON THE USE OF AN OSCILLATION-BASED TEST METHODOLOGY FOR CMOS MICRO-ELECTRO-MECHANICAL SYSTEMS
V Beroulle, Y Bertrand, L Latorre and P Nouet, LIRMM, FR

4D – 1 DIRECTED-BINARY SEARCH IN LOGIC BIST DIAGNOSTICS
R Kapur and T W Williams, Synopsys, US
M R Mercer, Texas A&M U, US

4D – 2 AN EVOLUTIONARY APPROACH TO THE DESIGN OF ON-CHIP PSEUDORANDOM TEST GENERATORS
M Favalli, DI- Ferrara U, IT
M Dalpasso, DEI – Padova U, IT

5D – 1 FAULT ISOLATION USING TESTS FOR NON-ISOLATED BLOCKS
I Pomeranz, Purdue U, US
Y Zorian, LogicVision, US

6D – 1 A HEURISTIC FOR TEST SCHEDULING AT SYSTEM LEVEL
M L Flottes, J Pouget and B Rouzeyre, LIRMM, FR

6D – 2 FORMULATION OF SoC TESTING SCHEDULING AS A NETWORK TRANSPORTATION PROBLEM
S Koranne and V Suhas, Philips, NL

8D – 1 A FAST JOHNSON-MOBIUS ENCODING SCHEME FOR FAULT SECURE BINARY COUNTERS
K S Papadomanolakis, A P Kakarountas, N Sklavos and C E Goutis, Patras U, GR

8D – 2 A NOVEL METHODOLOGY FOR THE CONCURRENT TEST OF PARTIAL AND DYNAMICALLY RECONFIGURABLE SRAM-BASED FPGAs
M G Gericota and G R Alves, ISEP, PT
M L Silva and J M Ferreira, FEUP/INESC, PT

8D – 3 EFFICIENT ON-LINE TESTING METHOD FOR A FLOATING-POINT ITERATIVE ARRAY DIVIDER
A Drozd, M Lobachev and J Drozd, Odessa State Polytechnic U, UKR

1E – 1 POWER MODELING AND REDUCTION OF VLIW PROCESSORS
W Liao and L He, Wisconsin U, Madison, US

1E – 2 AN INSTRUCTION-LEVEL METHODOLOGY FOR POWER ESTIMATION AND OPTIMIZATION OF EMBEDDED VLIW CORES
A Bona, M Sami, D Sciuto and V Zaccaria, Politecnico di Milano, IT
C Silvano, U degli Studi di Milano, IT
R Zafalon, STMicroelectronics

2E – 1 THE FRAUNHOFER KNOWLEDGE NETWORK (FKN) FOR TRAINING IN CRITICAL DESIGN DISCIPLINES
A Sauer and G Elst, FhG IIS/EAS, DE
L Krahn and W John, FhG IZM, DE

2E – 2 COMPARATIVE ANALYSIS AND APPLICATION OF DATA REPOSITORY INFRASTRUCTURE FOR COLLABORATION-ENABLED DISTRIBUTED DESIGN ENVIRONMENTS
L S Indrusiak, TU Darmstadt, DE/UFRGS, BRZ
M Glesner, TU Darmstadt, DE
R Reis, UFRGS, BRZ

3E – 1 AREA-EFFICIENT MEMORY FOR SELF-PROFILING MICROPROCESSOR PLATFORMS
S Cotterell, F Vahid and R Lysecky, UC Riverside, US

3E – 2 FlexBench: REUSE OF VERIFICATION IP TO INCREASE PRODUCTIVITY
S Stoehr, M Simmons and J Geishauser, Motorola Munich, DE

5E – 1 MAPPABILITY ESTIMATION OF ARCHITECTURE AND ALGORITHM
J-P Soininen, J Kreku and Y Qu, VTT Electronics, FI

6E – 1 BEHAVIOURAL MODELLING OF OPERATIONAL AMPLIFIER FAULTS USING VHDL-AMS
P R Wilson, J N Ross, M Zwolinski and A D Brown, Southampton U, UK
Y Kilic, Philips Semiconductors, UK

6E – 2 A PARALLEL LCC SIMULATION SYSTEM
K Hering, Chemnitz U, DE

6E – 3 ERROR SIMULATION BASED ON THE SystemC DESIGN DESCRIPTION LANGUAGE
F Bruschi, M Chiamenti, F Ferrandi and D Sciuto, Politecnico di Milano, IT

6E – 4 TOWARDS A KERNEL LANGUAGE FOR HETEROGENEOUS COMPUTING
D Björklund and J Lilius, Turku Center for Computer Science (TUCS), FI

8E – 1 TOP-DOWN SYSTEM LEVEL DESIGN METHODOLOGY USING SpecC, VCC AND SystemC
L Cai and D Gajski, UC Irvine, US
P Kritzinger and M Olivarez, Motorola, US

9E – 1 AUTOMATIC TOPOLOGY-BASED IDENTIFICATION OF INSTRUCTION-SET EXTENSIONS FOR EMBEDDED PROCESSORS
L Pozzi, M Vuletic and P Ienne, EPFL, CH

9E – 2 TUNING PLATFORMS WITH CONFIGURABLE VOLTAGE AND CACHE
T Givargis, UC Irvine, US
F Vahid and J Villarreal, UC Riverside, US

3F2 - 1 STEADY STATE CALCULATION OF OSCILLATORS USING CONTINUATION METHODS
H G Brachtendorf, S Lampe and R Laur, Bremen U, DE
R Melville, Agere Systems, US
P Feldmann, Celight Inc, US

FRIDAY 8 MARCH

MASTER COURSES – LEVEL 2

Master Course attendees should choose in advance one of either M1 or M2. The Master Courses run from 0830 in the morning until 1600 in the afternoon.

They will run in parallel with the following timescale and rooms will be signposted:

0730 - 0830	Registration and Master Course Buffet Breakfast
0830 – 1000	Master Courses – Level 2
1000 – 1015	Break
1015 - 1200	Master Courses – Level 2
1200 – 1300	Lunch – Level 4
1300 - 1430	Master Courses – Level 2
1430 - 1445	Break
1445 – 1600	Master Courses – Level 2
1600	CLOSE